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# CMOS single-chip 8-bit MCU with 12-bit A/D converter and LCD driver



## Main features

- **8-bit Microcontroller With High Speed 8051 CPU**
- **Basic MCU Function**
  - 24 Kbytes Flash Code Memory
  - 768 bytes SRAM(IRAM 256 bytes + XRAM 512 bytes)
- **Built-in Analog Function**
  - Power-On Reset and Low Voltage Detect Reset
  - Internal 8 MHz HFIRC Oscillator ( $\pm 1.0\%$ ,  $T_A = -10 \sim +55^\circ\text{C}$ , User trim)
  - Internal 32 kHz LFIRC Oscillator ( $\pm 5.0\%$ ,  $T_A = -10 \sim +55^\circ\text{C}$ )
  - Watchdog Timer RC Oscillator (5kHz)
- **Peripheral Features**
  - 12-bit Analog to Digital Converter (5 inputs)
  - LCD Driver (32 Segments x 8 Commons)
  - 16-bit CRC/Checksum Generator
  - Built-in Transistor for IR LED Drive
- **I/O and Packages**
  - 13 I/O, 46 Shared I/O with LCD signal
  - 64LQFP, 64QFN, 48LQFP, 48QFN
  - Pb-free package
- **Operating Conditions**
  - 1.8V to 5.5V Wide Voltage Range
  - $-40^\circ\text{C}$  to  $85^\circ\text{C}$  Temperature Range
- **Application**
  - Home appliance, Industrial Control

## A96R717

### Datasheet

V 1.4

Revised 7 September, 2018

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## Revision history

Version	Date	Revision list
1.0	2016.10.26	Published this book.
1.1	2016.10.31	Add a POR Hysteresis with 0.2V in 7.4 Power-On Reset Characteristics. Add '0.7/1.5 sec(@VDD=3V, TA=25°C)' to "sub oscillation stabilization time's typ/max value". Add a chapter 7.23 Recommended Circuit for remote controller.
1.2	2017.02.08	Updated Package diagrams in Chapter 4. Package Diagram. Added the IOH/IOL characteristics for normal I/O port in 7.11 DC Characteristics. Added notes about LVI in Chapter 13.8 LVI Block Diagram. Updated OCD dongle image in Chapter 1.3 Development tools.
1.3	2018.05.08	Updated 64-Pin LQFP-1010, 64-Pin QFN-0909, 48-Pin LQFP-0707, 48-Pin QFN-0707 Package diagram in Chapter 4. Package Diagram.
1.4	2018.09.07	Revised this book. Change Max and Min value of REM Output High Current in 7.11 DC Characteristics. Add Device Nomenclature. Add notes about External Interrupt register in Chapter 10.12.7 Register Description for Interrupt. More descriptions in Chapter 11.8.3 16-bit Capture Mode. Change Figure 11.31 16-Bit Capture Mode for Timer 3. Change Figure 11.34 16-Bit Timer 3 Block Diagram. Fix the typo.

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### Version 1.4

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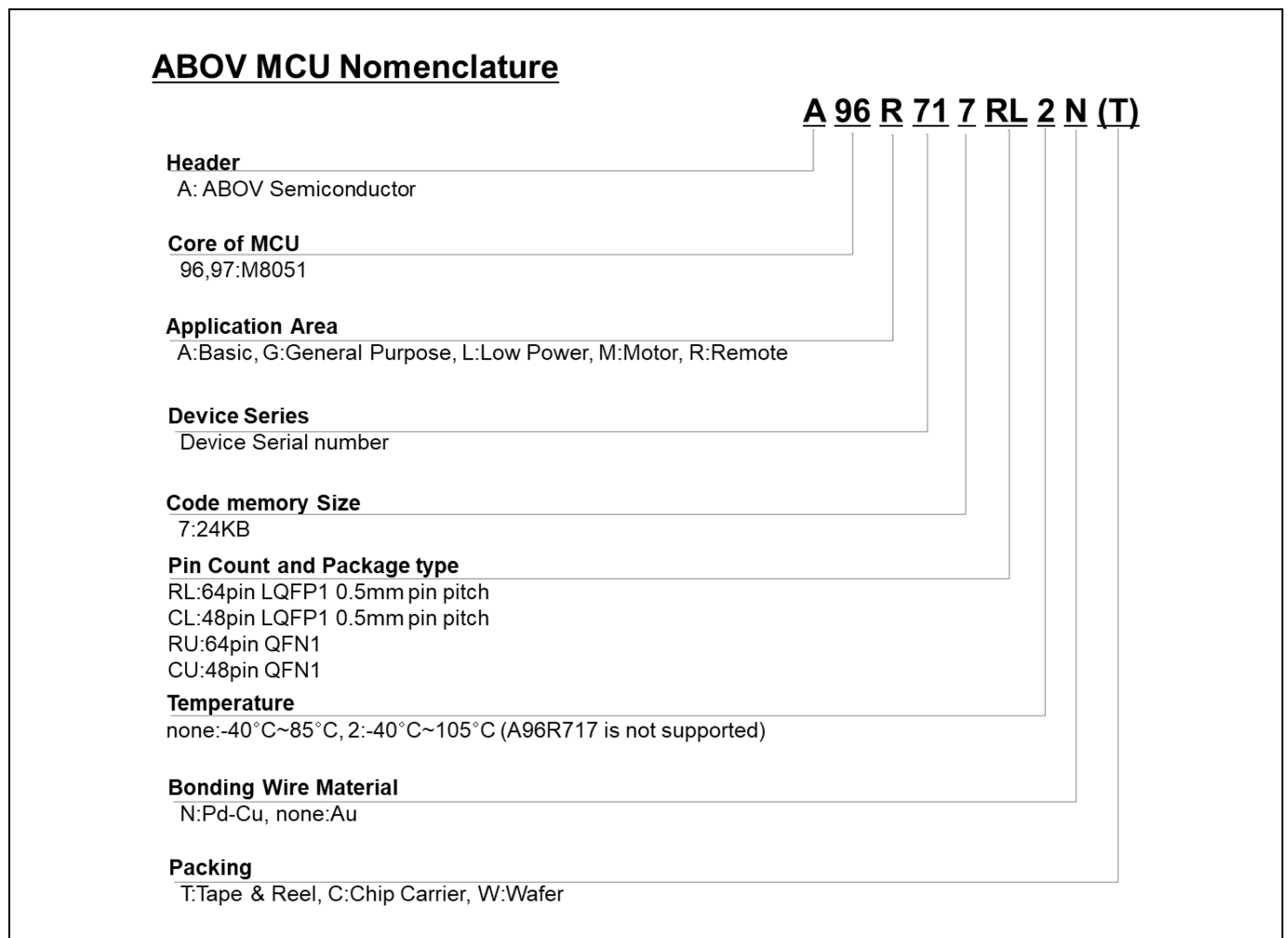
# 1 Overview

## 1.1 Description

The A96R717 is advanced CMOS 8-bit microcontroller with 24 Kbytes of FLASH. This is powerful microcontroller which provides a highly flexible and cost effective solution to many embedded control applications. This provides the following features : 24 Kbytes of FLASH, 256 bytes of IRAM, 512 bytes of XRAM, general purpose I/O, basic interval timer, watchdog timer, 8/16-bit timer/counter, carrier generation, watch timer, buzzer driving port, 12-bit A/D converter, LCD driver, 16-bit CRC/Checksum Generator, Built-in Transistor for I.R LED Drive, on-chip POR, LVR, LVI, on-chip oscillator and clock circuitry. The A96R717 also supports power down modes to reduce power consumption.

Device Name	FLASH	IRAM	XRAM	ADC	I/O PORT	Package
A96R717RL	24 Kbytes	256 bytes	512 bytes	5 inputs	59	64LQFP-1010
A96R717RU				5 inputs	59	64QFN-0909
A96R717CL				2 inputs	43	48LQFP-0707
A96R717CU				2 inputs	43	48QFN-0707

**Table 1.1** Ordering Information of A96R717



**Figure 1.1** Device Nomenclature

## 1.2 Features

- **CPU**
  - 8-bit CISC core (M8051, 2 clocks per cycle)
- **ROM (FLASH) Capacity**
  - 24 Kbytes Flash with self read/write capability
  - On Chip debug and In-System Programming(ISP)
  - Endurance : 10,000 times(Sector 0~379)  
100,000 times(Sector 380~383)
  - Retention : 10 years
- **256 bytes IRAM**
- **512 bytes XRAM**
  - 38 bytes including LCD display RAM
- **General Purpose I/O (GPIO)**
  - Normal I/O : 13 Ports  
(P4[7], P5[6:0], P6[4:0])
  - LCD shared I/O : 46 Ports  
(P0[7:0], P1[7:0], P2[7:0], P3[6:0], P4[6:0], P7[7:0])
- **Basic Interval Timer (BIT)**
  - 8-bitx 1-ch
- **Watch Dog Timer (WDT)**
  - 8-bitx 1-ch
  - 5kHz internal RC oscillator
- **Timer/Counter**
  - 8-bitx 2-ch(T0/T1), 16-bitx 2-ch (T2/T3)
  - 16-bit Interval Timer x 1ch
- **Carrier Generation**
  - Carrier generation (by T1), T3 Clock source
- **Programmable Pulse Generation**
  - Pulse generation (by T2/T3)
  - 8-Bit PWM (by T0)
- **Watch Timer (WT)**
  - 3.91ms/0.25s/0.5s/1s/1min interval at 32.768kHz
- **Buzzer**
  - 8-bitx 1-ch
- **UART**
  - 8-bitx 1-ch
- **12-bit A/D Converter**
  - 5 Input channels
- **LCD Driver**
  - 32 Segments and 8 Common
  - 1/2, 1/3, 1/4, 1/5, 1/6, 1/8 duty selectable
  - Voltage booster and 16-step contrast control
- **16-Bit CRC/Checksum Generator**
  - Auto and User CRC/Checksum mode
- **Built-in Transistor for I.R LED Drive**
  - IOL = 630mA at 3V and VOL = 1.0V
- **Power On Reset**
  - Reset release level (1.4V)
- **Low Voltage Reset**
  - 14 level detect (1.60/2.05/2.15/2.25/2.37/2.50/2.65/2.82/ 3.01/ 3.22/3.47/3.76/4.10/4.51V)
- **Low Current Low Voltage Reset**
  - 1.80V ± 90mV, 0.9uA Operating Current
- **Low Voltage Indicator**
  - 13 level detect (2.05/2.15/2.25/2.37/2.50/2.65/2.82/ 3.01/ 3.22/ 3.47/ 3.76/ 4.10/ 4.51V)
- **Interrupt Sources**
  - External Interrupts  
(EINT0 ~ EINT7, EINT10, EINT12, EINT13) (11)
  - Timer0/1/2/3 (5), Interval Timer (1)
  - WDT (1), BIT (1), WT (1)
  - ADC (1), UART (2), LVI (1)
- **Internal RC Oscillator**
  - HFIRC frequency:  
8MHz ±1.0% (T<sub>A</sub>= -10 ~ +55°C, User trim)
  - LFIRC frequency:  
32kHz ±5.0% (T<sub>A</sub>= -10 ~ +55°C)
- **Power Down Mode**
  - STOP, IDLE mode
- **Operating Voltage and Frequency**
  - 1.8V ~ 5.5V (@ 32 ~ 38kHz with SX-tal)
  - 2.0V ~ 5.5V (@ 0.4 ~ 4.2MHz with X-tal, Crystal)
  - 1.8V ~ 5.5V (@ 0.4 ~ 4.2MHz with X-tal, Ceramic)
  - 2.4V ~ 5.5V (@ 0.4 ~ 8.0MHz with X-tal)
  - 3.0V ~ 5.5V (@ 0.4 ~ 12.0MHz with X-tal)
  - 1.8V ~ 5.5V (@ 0.5MHz ~ 8MHz with HFIRC)
  - 1.8V ~ 5.5V (@ 4kHz ~ 32kHz with LFIRC)
  - Voltage dropout converter included for core
- **Minimum Instruction Execution Time**
  - 167ns (@12MHz main clock)
  - 61us (@ 32.768kHz sub clock)
- **Operating Temperature**
  - -40 ~ +85°C
- **Oscillator Type**
  - 0.4-12MHz Crystal or Ceramic for main clock
  - 32.768kHz Crystal for sub clock
- **Package Type**
  - 64-Pin LQFP-1010/48-Pin LQFP-0707
  - 64-Pin QFN-0909/48-Pin QFN-0707
  - Pb-free package

### 1.3 Development tools

#### 1.3.1 Compiler

We do not provide the compiler. Please contact the third parties.

The core of A96R717 is Mentor 8051. And, device ROM size is smaller than 64k bytes. Developer can use all kinds of third party's standard 8051 compiler.

#### 1.3.2 OCD(On-chip debugger) emulator and debugger

The OCD (On Chip Debug) emulator supports ABOV Semiconductor's 8051 series MCU emulation.

The OCD interface uses two-wire interfacing between PC and MCU which is attached to user's system. The OCD can read or change the value of MCU internal memory and I/O peripherals. And the OCD also controls MCU internal debugging logic, it means OCD controls emulation, step run, monitoring, etc.

The OCD Debugger program works on Microsoft-Windows NT, 2000, XP, Vista (32bit) operating system.

If you want to see more details, please refer to OCD debugger manual. You can download debugger S/W and manual from our web-site(<http://www.abov.co.kr>).

Connection:

- DSCL (A96R717 P33 port)
- DSDA (A96R717 P32 port)

OCD connector diagram: Connect OCD with user system

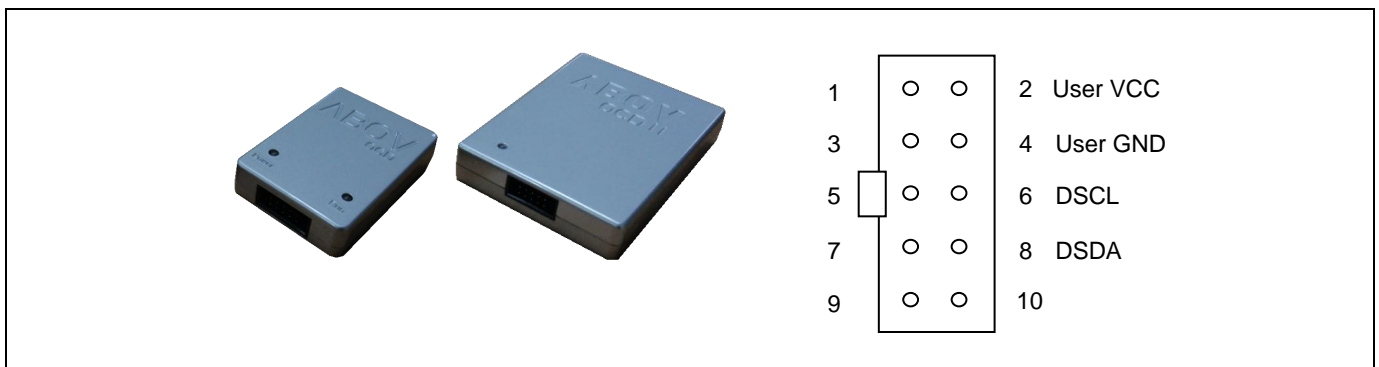


Figure 1.2 Debugger(OCD1/OCD2) and Pin description

### 1.3.3 Programmer

Single programmer :

E-PGM+ : It programs MCU device directly.

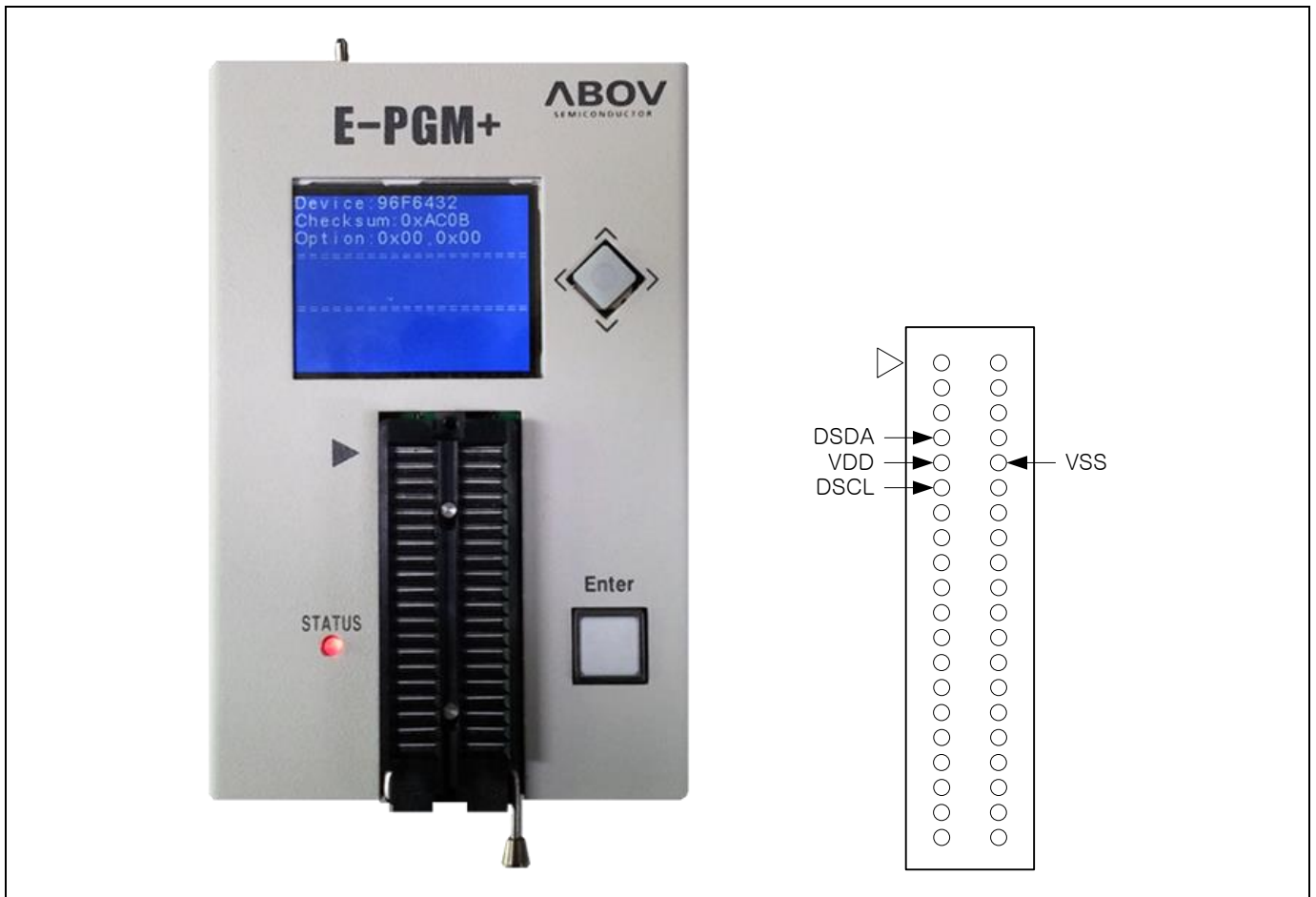


Figure 1.3 E-PGM+(Single writer)

OCD emulator:

It can write code to MCU device too, because OCD debugger supports ISP (In System Programming).It does not require additional H/W, except developer's target system.

Gang programmer: E-GANG4 and E-GANG6

- It can run PC controlled mode.
- It can run standalone without PC control too.
- USB interface is supported.
- Easy to connect to the handler.



**Figure 1.4** E-GANG4 and E-GANG6 (for Mass Production)

## 1.4 MTP programming

### 1.4.1 Overview

The program memory of A96R717 is MTP Type. This flash is accessed by serial data format. There are four pins(DSCL, DSDA, VDD, VSS) for programming/reading the flash.

Pin name	Main chip pin name	During programming	
		I/O	Description
DSCL	P33	I	Serial clock pin. Input only pin.
DSDA	P32	I/O	Serial data pin. Output port when reading and input port when programming. Can be assigned as input/push-pull output port.
VDD, VSS	VDD, VSS	-	Logic power supply pin.

**Table 1.2** Descriptions of pins which are used to programming/reading the Flash

### 1.4.2 On-Board programming

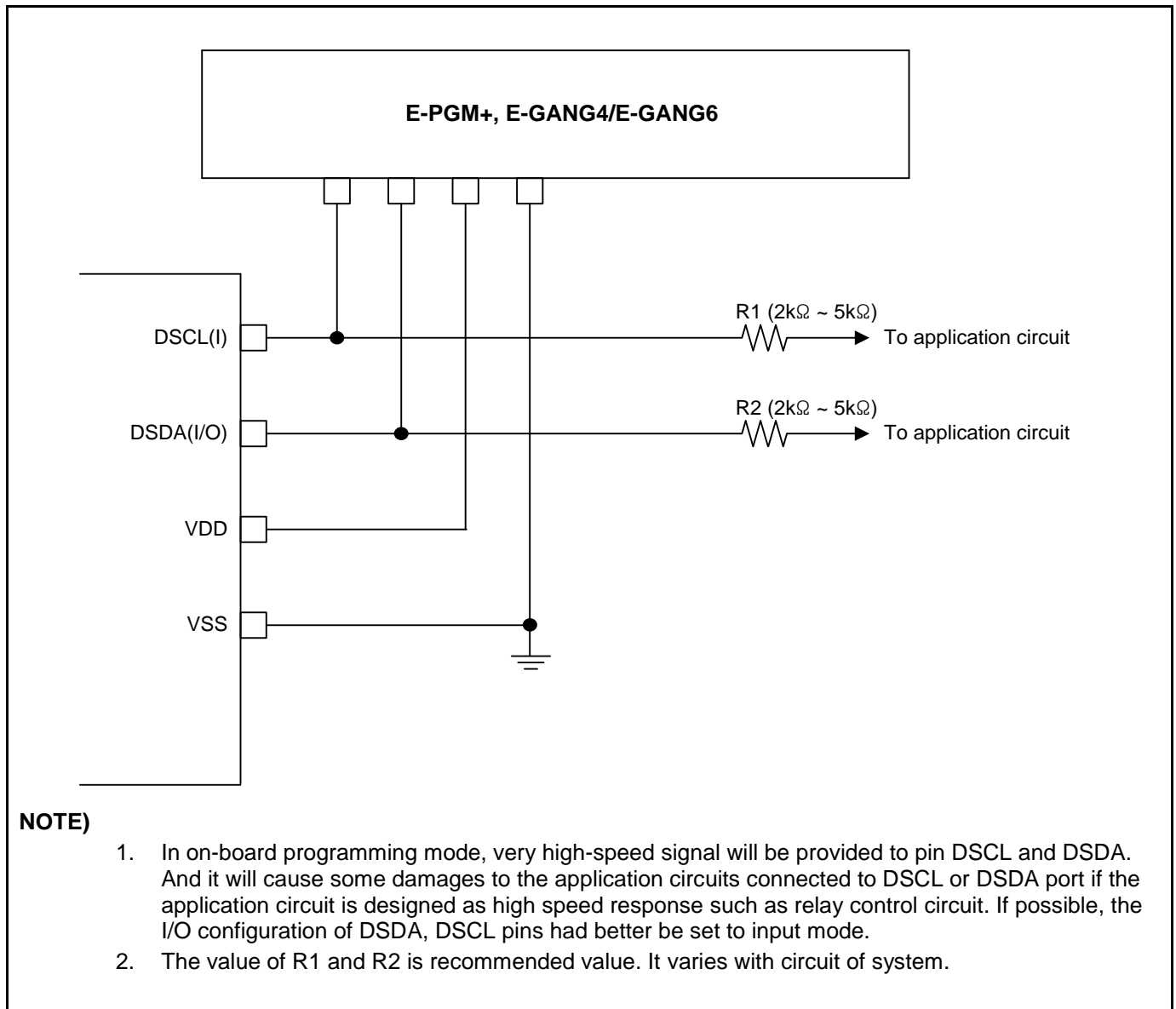
The A96R717 needs only four signal lines including VDD and VSS pins for programming FLASH with serial protocol. Therefore the on-board programming is possible if the programming signal lines are considered when the PCB of application board is designed.



### 1.4.3 Circuit Design Guide

At the FLASH programming, the programming tool needs 4 signal lines that are DSCL, DSDA, VDD and VSS. When you design the PCB circuits, you should consider the usage of these signal lines for the on-board programming.

Please be careful to design the related circuit of these signal pins because rising/falling timing of DSCL and DSDA is very important for proper programming.



**Figure 1.5** PCB design guide for on board programming

## 2 Block diagram

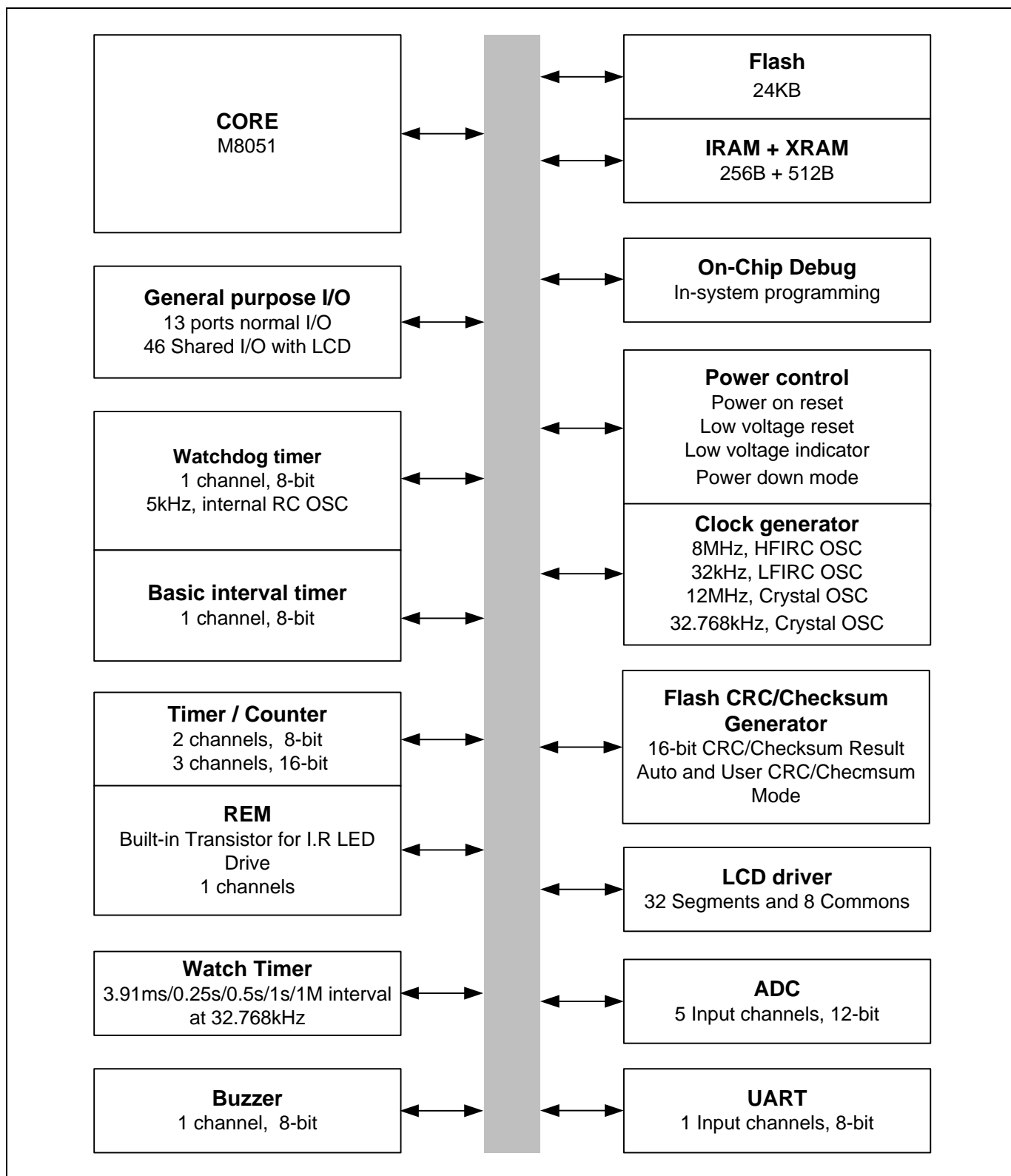


Figure 2.1 Block diagram of A96R717

### 3 Pin assignment

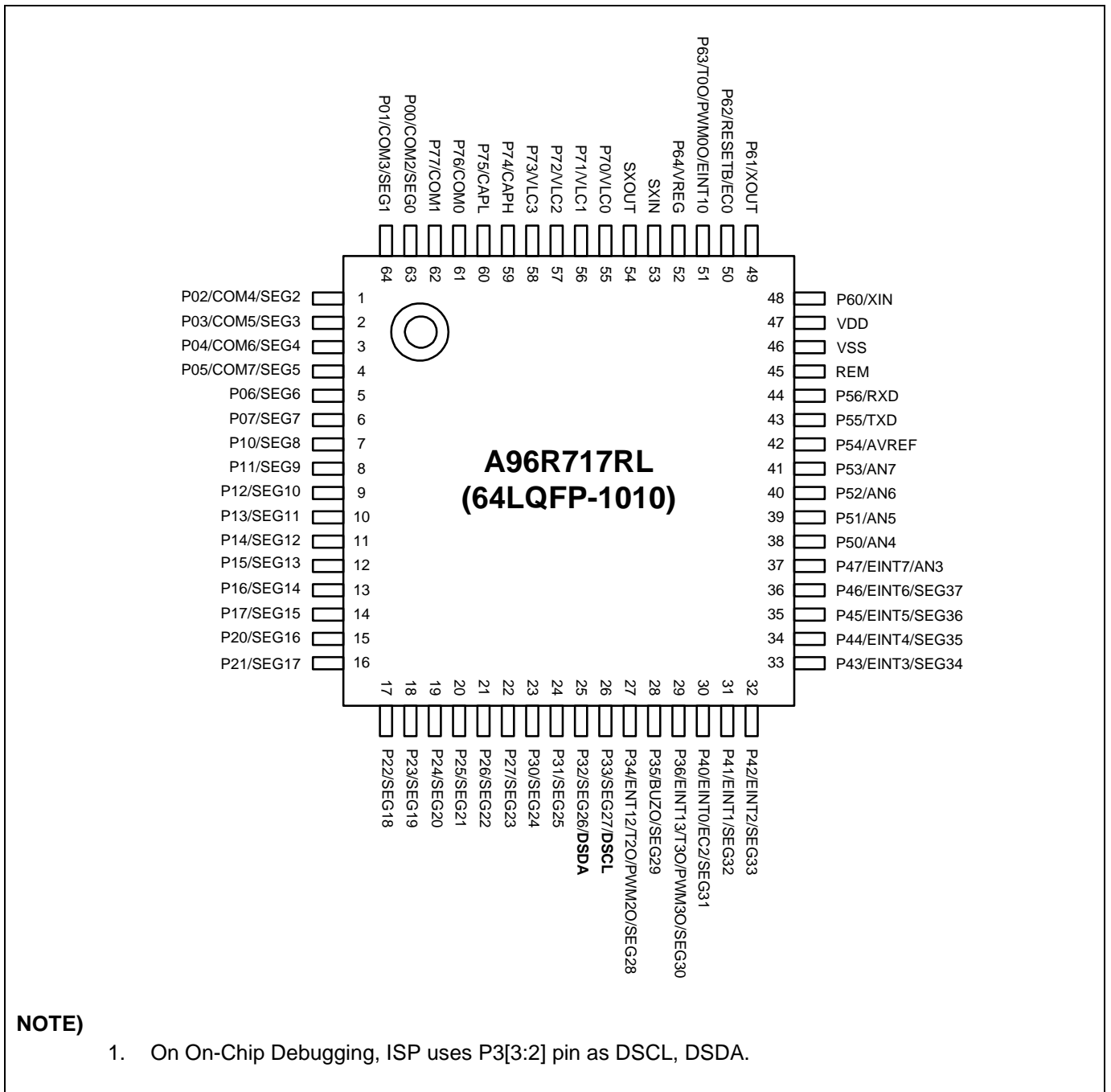
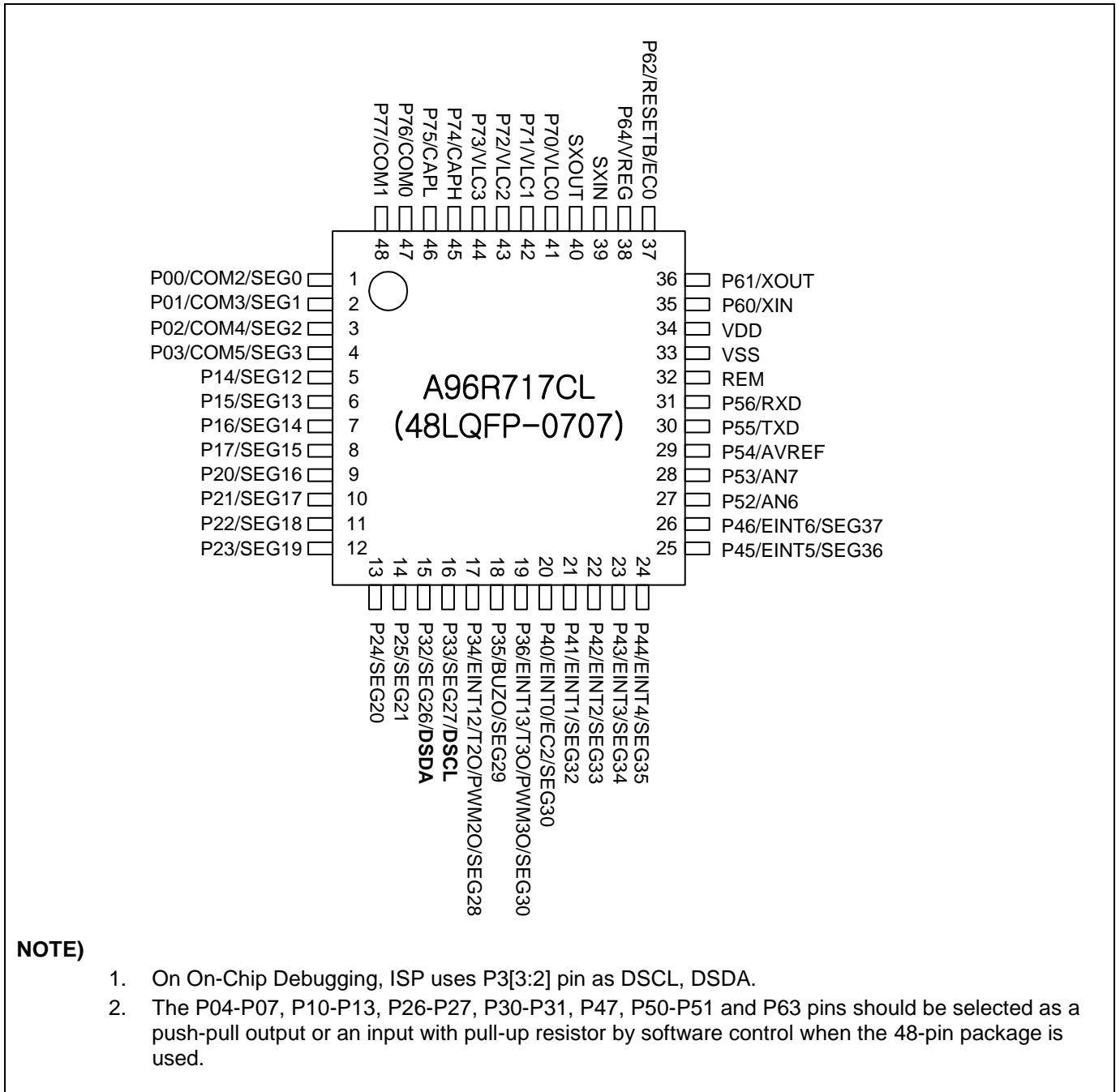


Figure 3.1 A96R717RL 64LQFP Pin Assignment





**NOTE)**

1. On On-Chip Debugging, ISP uses P3[3:2] pin as DSCL, DSDA.
2. The P04-P07, P10-P13, P26-P27, P30-P31, P47, P50-P51 and P63 pins should be selected as a push-pull output or an input with pull-up resistor by software control when the 48-pin package is used.

**Figure 3.3** A96R717CL 48LQFP Pin Assignment



# 4 Package Diagram

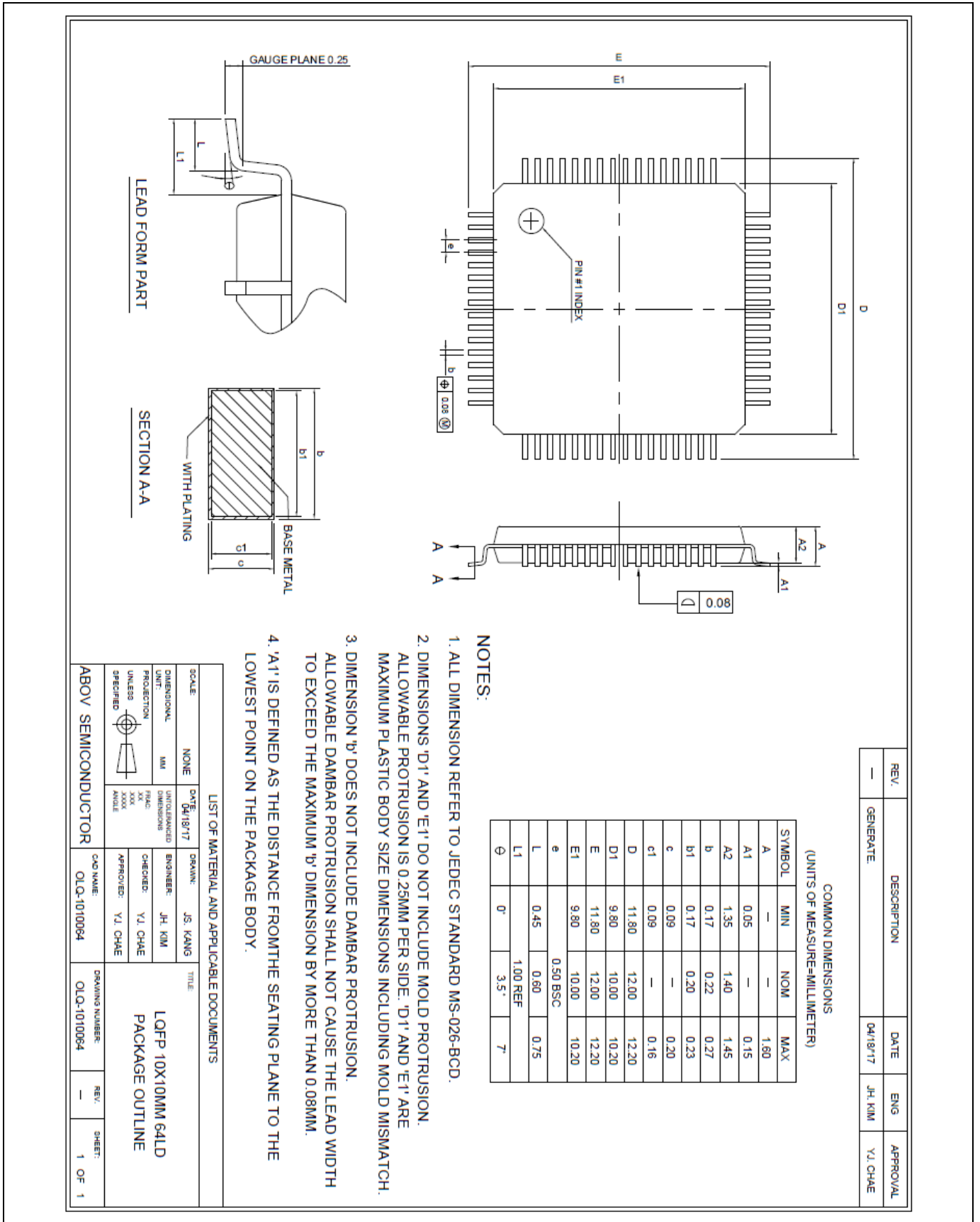
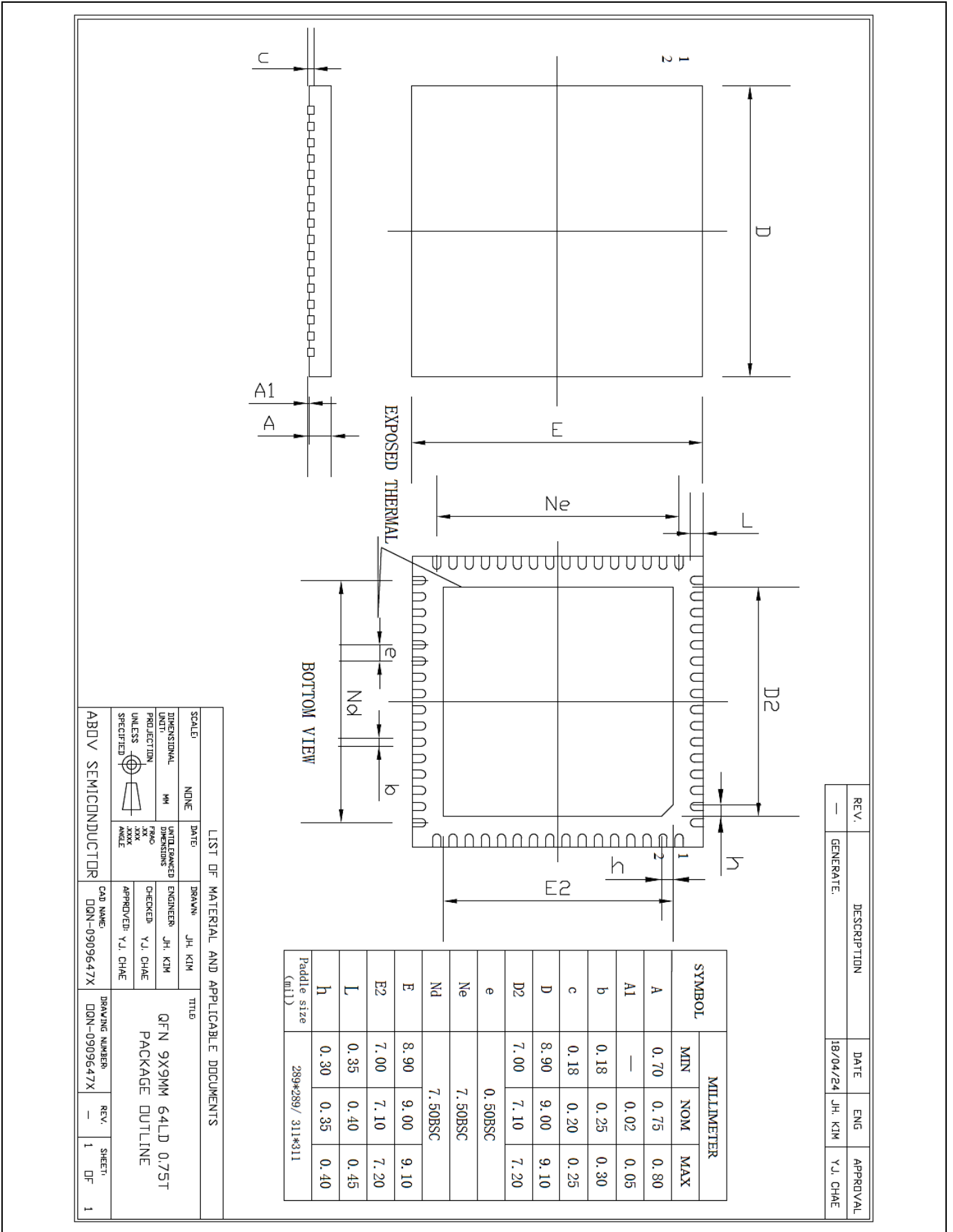


Figure 4.1 64-Pin LQFP-1010 Package



LIST OF MATERIAL AND APPLICABLE DOCUMENTS

SCALE	NONE	DATE	DRAWN	JH. KIM	TITLE				
DIMENSIONAL UNIT	MM	UNTOLENCED DIMENSIONS	ENGINEER	JH. KIM	QFN 9X9MM 64LD 0.75T PACKAGE OUTLINE				
PROJECTION	FRMO XXX XXXX	CHECKED	YJ. CHAE	YJ. CHAE					
UNLESS SPECIFIED	ANGLE	APPROVED	YJ. CHAE						
		CAD NAME	DDN-0909647X	DRAWING NUMBER		DDN-0909647X			
ABOV SEMICONDUCTOR				REV.	—	SHEET	1	OF	1

REV.	DESCRIPTION	DATE	ENG	APPROVAL
—	GENERATE.	18/04/24	JH. KIM	YJ. CHAE

Figure 4.2 64-Pin QFN-0909 Package



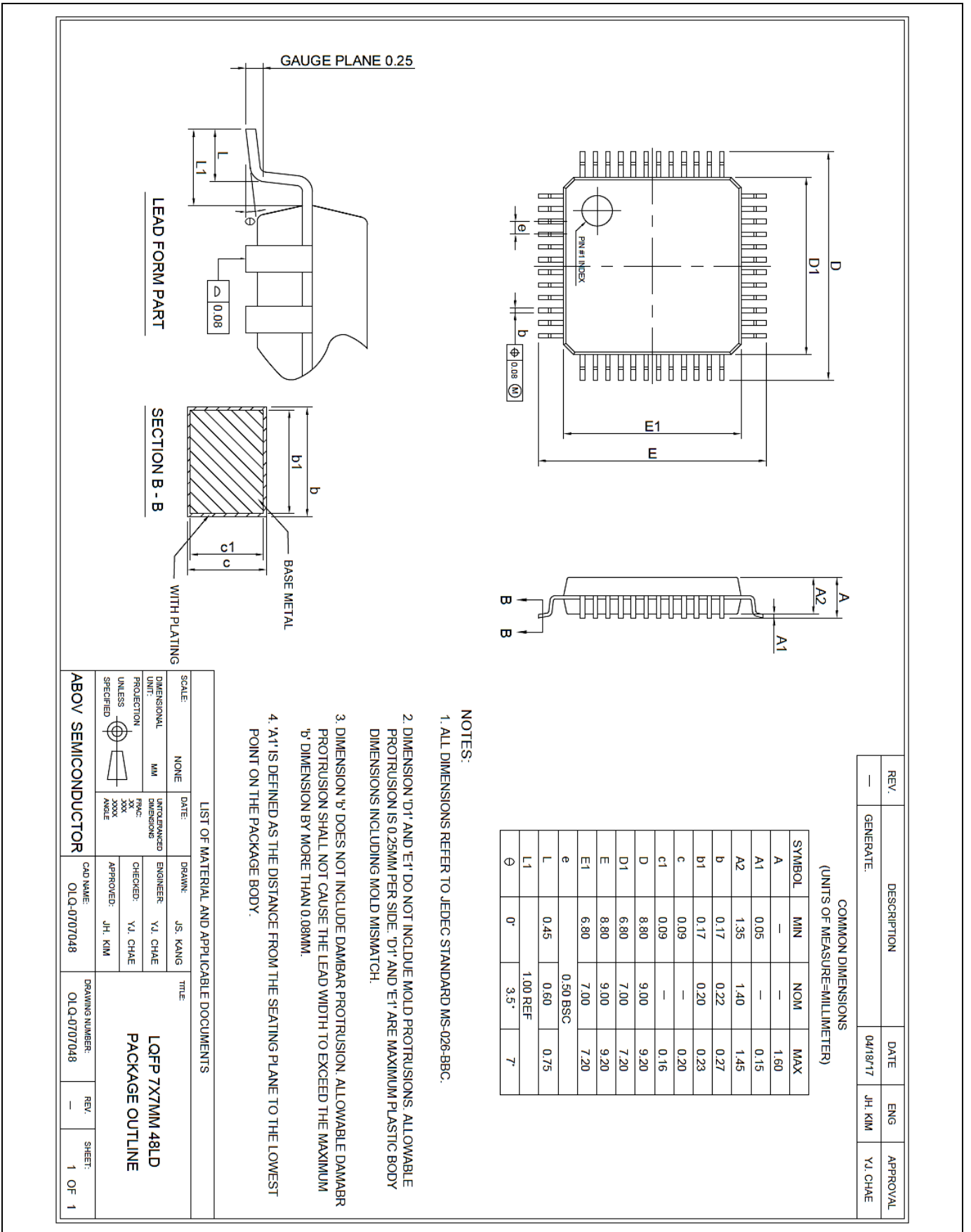
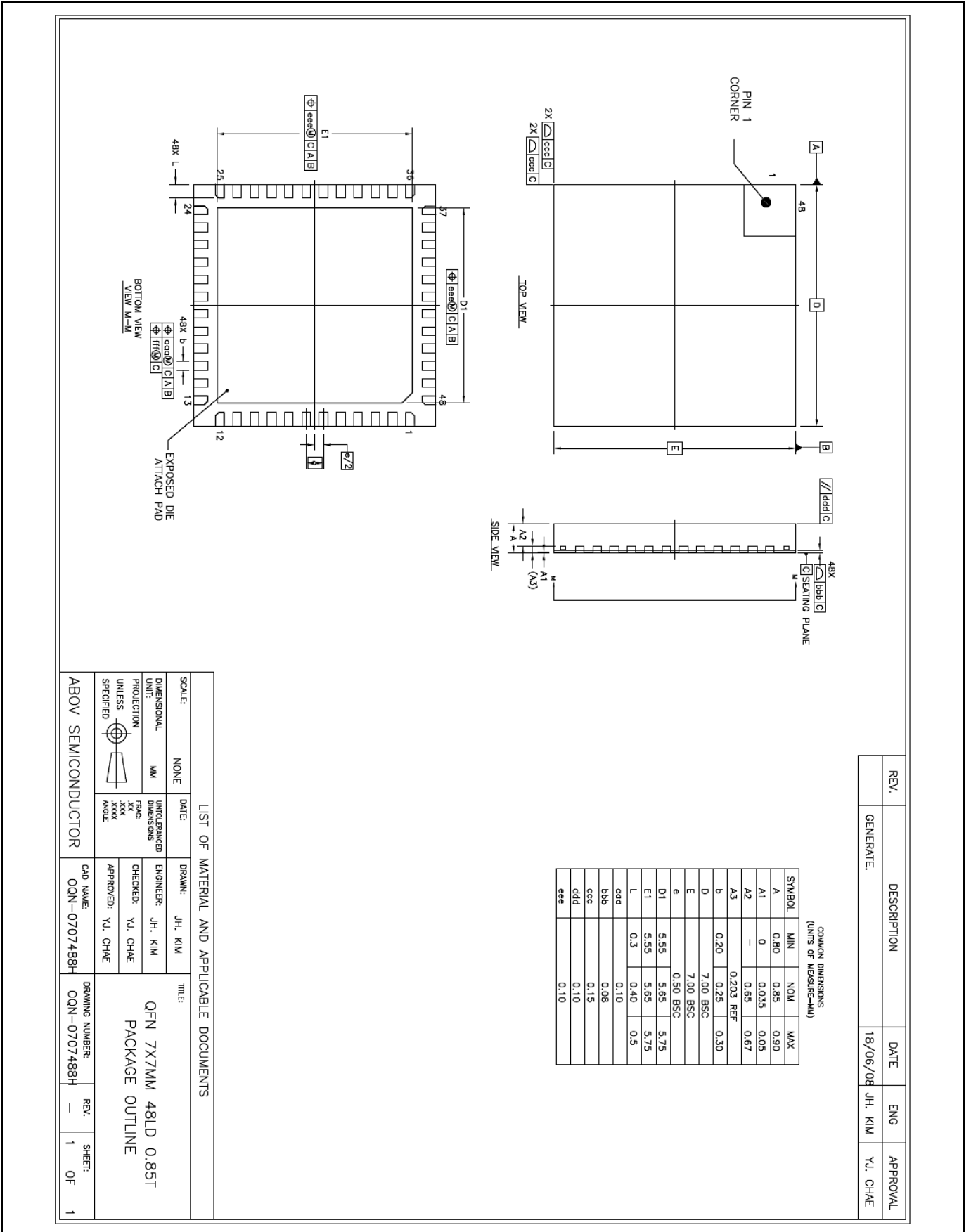


Figure 4.3

48-Pin LQFP-0707 Package



LIST OF MATERIAL AND APPLICABLE DOCUMENTS			
SCALE: NONE	DATE: UNRENDERED DIMENSIONS	DRWGN: JH. KIM	TITLE: QFN 7X7MM 48LD 0.85T PACKAGE OUTLINE
DIMENSIONAL UNIT: MM	PROJECTION: UNLESS SPECIFIED	ENGINEER: JH. KIM	
		CHECKED: YJ. CHAE	
		APPROVED: YJ. CHAE	
ABOV SEMICONDUCTOR		CAD NAME: QQN-070748BH	DRAWING NUMBER: QQN-070748BH
		REV: 1	SHEET: 1 OF 1

REV.	DESCRIPTION	DATE	ENG	APPROVAL
GENERATE		18/06/08	JH. KIM	YJ. CHAE

Figure 4.4 48-Pin QFN-0707 Package

## 5 Pin Description

PIN Name	I/O	Function	@RESET	Shared with
P00	I/O	Port 0 is a bit-programmable I/O port which can be configured as an input, a push-pull output or an open-drain output. A pull-up resistor can be specified in 1-bit unit. The P04–P07 are not in the 48-Pin package.	Input	COM2/SEG0
P01				COM3/SEG1
P02				COM4/SEG2
P03				COM5/SEG3
P04				COM6/SEG4
P05				COM7/SEG5
P06				SEG6
P07				SEG7
P10	I/O	Port 1 is a bit-programmable I/O port which can be configured as an input, a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit. The P10–P13 are not in the 48-Pin package.	Input	SEG8
P11				SEG9
P12				SEG10
P13				SEG11
P14				SEG12
P15				SEG13
P16				SEG14
P17				SEG15
P20	I/O	Port 2 is a bit-programmable I/O port which can be configured as an input, a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit. The P26–P27 are not in the 48-Pin package.	Input	SEG16
P21				SEG17
P22				SEG18
P23				SEG19
P24				SEG20
P25				SEG21
P26				SEG22
P27				SEG23
P30	I/O	Port 3 is a bit-programmable I/O port which can be configured as an input (P32 – P36: Schmitt trigger input), a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit. The P30–P31 are not in the 48-Pin package.	Input	SEG24
P31				SEG25
P32				SEG26/DSDA
P33				SEG27/DSCL
P34				ENIT12/T20/PWM20/SEG28
P35				BUZO/SEG29
P36				EINT13/T30/PWM30/SEG30
P40				I/O
P41	EINT1/SEG32			
P42	EINT2/SEG33			
P43	EINT3/SEG34			
P44	EINT4/SEG35			
P45	EINT5/SEG36			
P46	EINT6/SEG37			
P47	EINT7/AN3			

**Table 5.1** Normal Pin Description

PIN Name	I/O	Function	@RESET	Shared with
P50	I/O	Port 5 is a bit-programmable I/O port which can be configured as a schmitt-trigger input, a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit. The P50–P51 is not in the 48-Pin package.	Input	AN4
P51				AN5
P52				AN6
P53				AN7
P54				AVREF
P55				TXD
P56				RXD
P60	I/O	Port 6 is a bit-programmable I/O port which can be configured as a schmitt-trigger input, a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit. The P63 are not in the 48-Pin package.	Input	XIN
P61				XOUT
P62				RESETB/EC0
P63				T00/PWM00/ENT10
P64				VREG
P70	I/O	Port 7 is a bit-programmable I/O port which can be configured as an input, a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit.	Input	VLC0
P71				VLC1
P72				VLC2
P73				VLC3
P74				CAPL
P75				CAPH
P76				COM0
P77				COM1
EINT10	I/O	External interrupt and Timer 0 capture input	Input	P63/T00/PWM00
EINT12	I/O	External interrupt and Timer 2 capture input	Input	P34/T20/PWM20/SEG28
EINT13	I/O	External interrupt and Timer 3 capture input	Input	P36/T30/PWM30/SEG30
EINT0	I/O	External interrupt inputs	Input	P40/EC2/SEG31
EINT1				P41/SEG32
EINT2				P42/SEG33
EINT3				P43/SEG34
EINT4				P44/SEG35
EINT5				P45/SEG36
EINT6				P46/SEG37
EINT7				P47/AN3
T00	I/O	Timer 0 interval output	Input	P63/PWM00/EINT10
T20	I/O	Timer 2 interval output	Input	P34/PWM20/ENIT12/SEG28
T30	I/O	Timer 3 interval output	Input	P36/PWM30/ENIT13/SEG30
PWM00	I/O	Timer 0 PWM output	Input	P63/T00/EINT10
PWM20	I/O	Timer 2 pulse output	Input	P34/T20/ENT12/SEG28
PWM30	I/O	Timer 3 pulse output	Input	P36/T30/ENT13/SEG30
EC0	I/O	Timer 0 event count input	Input	P62/RESETB
EC2	I/O	Timer 2 event count input	Input	P40/EINT0/SEG31
REM	O	High current n-channel open-drain output for driving I.R. LED.	Output	–
BUZO	I/O	Buzzer signal output	Input	P35/SEG29
TXD	I/O	UART data output	Input	P55
RXD	I/O	UART data input	Input	P56

Table 5.1 Normal Pin Description (Continued)

PIN Name	I/O	Function	@RESET	Shared with
AN3	I/O	A/D converter analog input channels	Input	P47/EINT7
AN4				P50
AN5				P51
AN6				P52
AN7				P53
VLC0–VLC3	I/O	LCD bias voltage pins	Input	P70–P73
CAPH	I/O	Capacitor terminals for voltage booster	Input	P74
CAPL			Input	P75
COM0	I/O	LCD common signal outputs	Input	P76
COM1				P77
COM2				P00/SEG0
COM3				P01/SEG1
COM4				P02/SEG2
COM5				P03/SEG3
COM6				P04/SEG4
COM7				P05/SEG5
SEG0	I/O	LCD segment signal outputs	Input	P00/COM2
SEG1				P01/COM3
SEG2				P02/COM4
SEG3				P03/COM5
SEG4				P04/COM6
SEG5				P05/COM7
SEG6				P06
SEG7				P07
SEG8–SEG15				P10–P17
SEG16–SEG23				P20–P27
SEG24				P30
SEG25				P31
SEG26				P32/DSDA
SEG27				P33/DSCL
SEG28				P34/EINT12/T2O/PWM2O
SEG29				P35/BUZO
SEG30				P36/EINT13/T3O/PWM3O
SEG31				P40/EINT0/EC2
SEG32				P41/EINT1
SEG33				P42/EINT2
SEG34				P43/EINT3
SEG35				P44/EINT4
SEG36				P45/EINT5
SEG37				P46/EINT6

**Table 5.1** Normal Pin Description (Continued)

PIN Name	I/O	Function	@RESET	Shared with
RESETB	I/O	System reset pin with a pull-up resistor when it is selected as the RESETB by "CONFIGURE OPTION"	Input	P62/EC0
DSDA	I/O	On chip debugger data input/output	Input	P32/SEG26
DSCL	I/O	On chip debugger clock input	Input	P33/SEG27
XIN	I/O	Main oscillator pins	Input	P60
XOUT				P61
SXIN, SXOUT	I/O	Sub oscillator pins	Input	–
VREG	I/O	Regulator voltage output for sub clock. 0.1uF capacitor needed.	Input	P64
AVREF	I/O	A/D converter reference voltage	Input	P54
VDD, VSS	–	Power input pins	–	–

**Table 5.1** Normal Pin Description (Concluded)

**NOTE)**

1. The P62/RESETB/EC0 pin is configured as one of the P62/EC0 and the RESETB pin by the "CONFIGURE OPTION".
2. If the P32/SEG26/DSDA and P33/SEG27/DSCL pins are connected to an emulator during reset or power-on reset, the pins are automatically configured as the debugger pins.
3. The P32/SEG26/DSDA and P33/SEG27/DSCL pins are configured as inputs with an internal pull-up resistor only during the reset or power-on reset.
4. The P60/XIN and P61/XOUT pins are configured as a function pin by software control.
5. The P64/VREG pins are configured as a function pin by software control.
6. The P64/VREG pin should be configured as a VREG alternative function if a sub oscillator is used.
7. The P04-P07, P10-P13, P26-P27, P30-P31, P47, P50-P51 and P63 are not in the 48-pin package.

## 6 Port Structures

### 6.1 General Purpose I/O Port

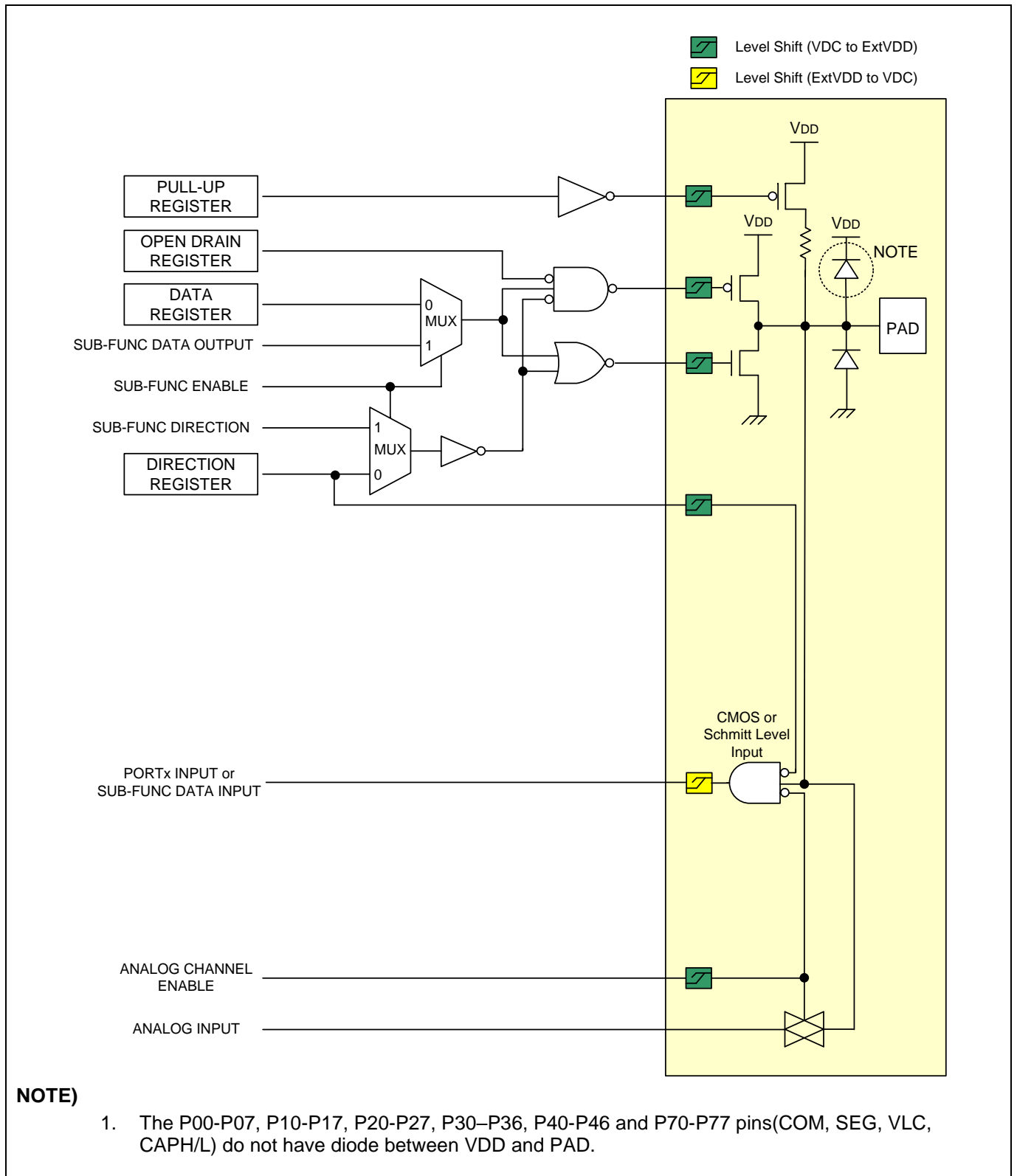


Figure 6.1 General Purpose I/O Port

## 6.2 External Interrupt I/O Port

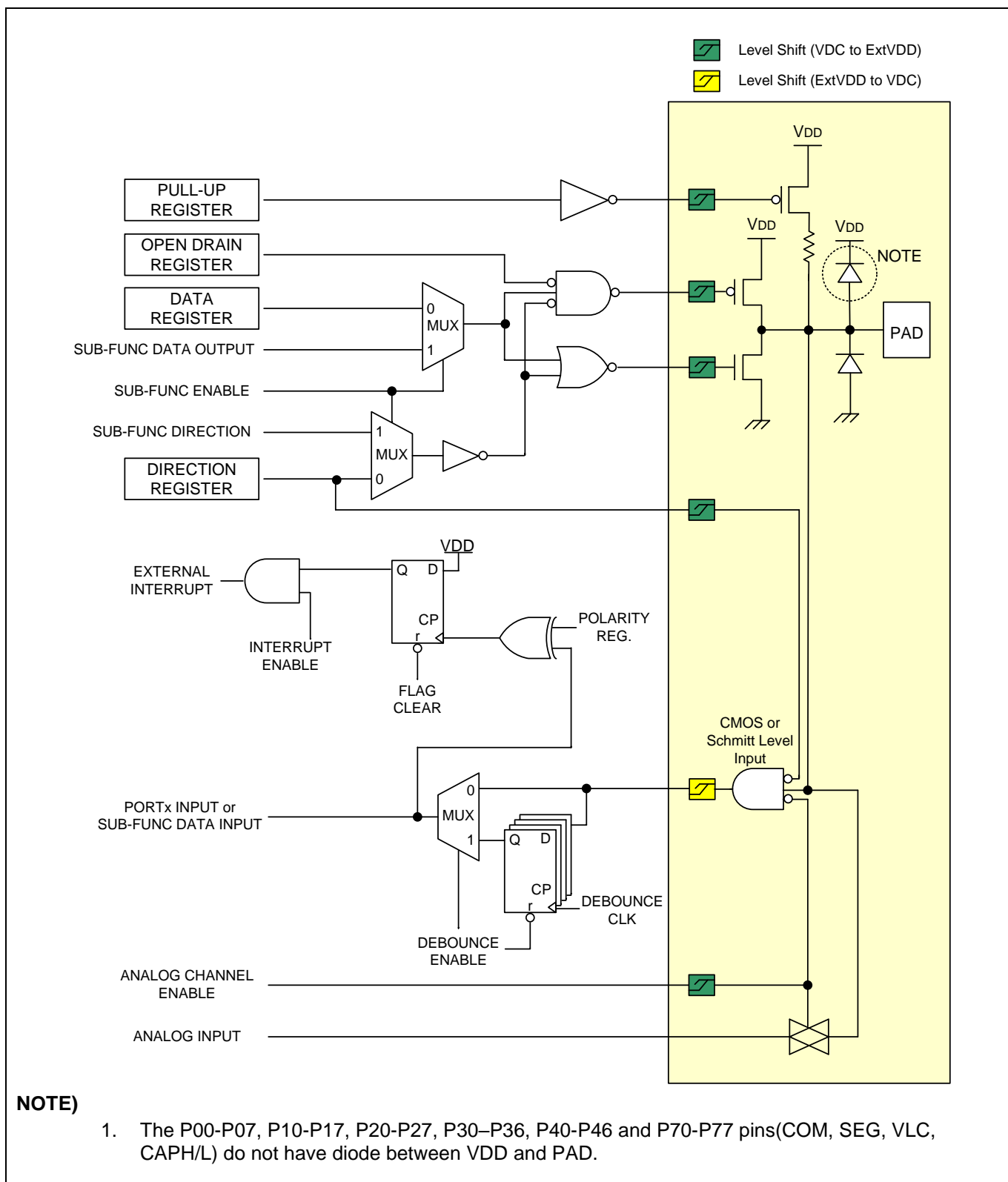


Figure 6.2 External Interrupt I/O Port



## 7 Electrical Characteristics

### 7.1 Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit	Note
Supply Voltage	VDD	-0.3 – +6.5	V	–
Normal Pin	V <sub>I</sub>	-0.3 – VDD+0.3	V	Voltage on any pin with respect to V <sub>SS</sub>
	V <sub>O</sub>	-0.3 – VDD+0.3	V	
	I <sub>OH</sub>	-10	mA	Maximum current output sourced by (I <sub>OH</sub> per I/O pin)
	∑ I <sub>OH</sub>	-80	mA	Maximum current (∑ I <sub>OH</sub> )
	I <sub>OL</sub>	60	mA	Maximum current sunk by (I <sub>OL</sub> per I/O pin)
	∑ I <sub>OL</sub>	120	mA	Maximum current (∑ I <sub>OL</sub> )
REM Output Pin	I <sub>OL</sub>	800	mA	Maximum current sunk by REM pin
Total Power Dissipation	P <sub>T</sub>	600	mW	–
Storage Temperature	T <sub>STG</sub>	-65 – +150	°C	–

**Table 7.1** Absolute Maximum Ratings

#### NOTE)

- Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### 7.2 Recommended Operating Conditions

Parameter	Symbol	Conditions		(T <sub>A</sub> =-40°C ~ +85°C)		Units	
				Min	Max		
Operating Voltage	VDD	fx = 32 – 38kHz	SX-tal	1.8	5.5	V	
		fx = 0.4 – 4.2MHz	X-tal	Ceramic	1.8		5.5
				Crystal	2.0		5.5
		fx = 0.4 – 8MHz	X-tal	2.4	5.5		
		fx = 0.4 – 12MHz		3.0	5.5		
		fx = 0.5 – 8MHz	HFIRC	1.8	5.5		
fx = 4.0 – 32kHz	LFIRC	1.8	5.5				
Operating Temperature	T <sub>OPR</sub>	VDD = 1.8 – 5.5V		-40	85	°C	

**Table 7.2** Recommended Operating Conditions

### 7.3 A/D Converter Characteristics

(T<sub>A</sub>=-40°C ~ +85°C, VDD=1.8V ~ 5.5V, VSS=0V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units	
Resolution	–	–	–	12	–	bit	
Integral Non-Linear	INL	AVREF=2.7V – 5.5V, fx=8MHz	–	–	±6	LSB	
Differential Non-Linearity	DNL		–	–	±1		
Top Offset Error	TOE		–	–	±5		
Zero Offset Error	ZOE		–	–	±5		
Conversion Time	t <sub>CONV</sub>	AVREF=4.0V – 5.5V	20	–	–	us	
		AVREF=3.0V – 5.5V	30	–	–		
		AVREF=2.7V – 5.5V	60	–	–		
Analog Input Voltage	V <sub>AIN</sub>	–	VSS	–	AVREF	V	
Analog Reference Voltage	AVREF	–	1.8	–	VDD		
A/DC Input Leakage Current	I <sub>AIN</sub>	AVREF=5.12V	–	–	10	uA	
A/DC Current	I <sub>ADC</sub>	Enable	VDD=5.12V	–	1	2	mA
		Disable		–	–	0.1	uA

**Table 7.3** A/D Converter Characteristics

**NOTE)**

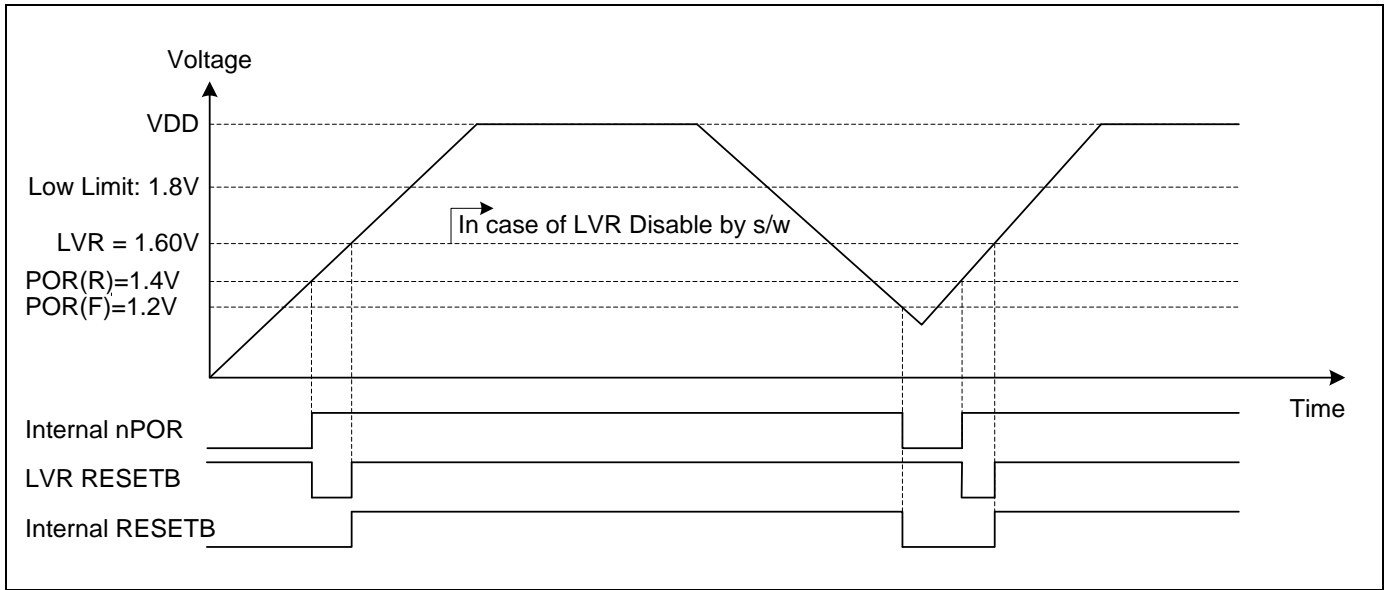
1. Zero offset error is the difference between 000000000000 and the converted output for zero input voltage (VSS).
2. Top offset error is the difference between 111111111111 and the converted output for top input voltage (AVREF).
3. If AVREF is less than 2.7V, the resolution degrades by 1-bit whenever AVREF drops 0.1V. (@ADCLK = 0.5MHz, Under 2.7V resolution has no test.)

### 7.4 Power-On Reset Characteristics

( $T_A = -40^{\circ}\text{C} \sim +85^{\circ}\text{C}$ ,  $V_{DD} = 1.8\text{V} \sim 5.5\text{V}$ ,  $V_{SS} = 0\text{V}$ )

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Reset Release Level	$V_{POR}$	-	-	1.4	-	V
Hysteresis	$\Delta V$	-	-	0.2	-	V
VDD Voltage Rising Time	$t_R$	0.5V – 2.0V	0.05	-	30.0	V/ms
POR Current	$I_{POR}$	-	-	0.2	-	$\mu\text{A}$

**Table 7.4** Power-on Reset Characteristics



**Figure 7.1** Power-on Reset Timing

### 7.5 Low Voltage Reset and Low Voltage Indicator Characteristics

(T<sub>A</sub>=-40°C ~ +85°C, VDD=1.8V ~ 5.5V, VSS=0V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units	
Detection Level	V <sub>LVR</sub> V <sub>LVI</sub>	The LVR can select all levels but LVI can select other levels except 1.60V.	-	1.60	1.79	V	
			1.90	2.05	2.20		
			2.00	2.15	2.30		
			2.10	2.25	2.40		
			2.22	2.37	2.52		
			2.35	2.50	2.65		
			2.45	2.65	2.85		
			2.62	2.82	3.02		
			2.81	3.01	3.21		
			3.02	3.22	3.42		
			3.27	3.47	3.67		
			3.46	3.76	4.06		
			3.80	4.10	4.40		
4.21	4.51	4.81					
LVR Hysteresis	ΔV	-	-	50	150	mV	
LVI Hysteresis	ΔV	-	-	10	100		
Minimum Pulse Width	t <sub>LOW</sub>	-	100	-	-	us	
LVR and LVI Current	I <sub>BL</sub>	Enable (Both)	VDD=3V, Run mode	-	14.0	24.0	uA
		Enable (One of two)		-	10.0	18.0	
		Disable (Both)		VDD=3V	-	-	

**Table 7.5** LVR and LVI Characteristics

### 7.6 Low Current Low Voltage Reset Characteristics

(T<sub>A</sub>=-40°C ~ +85°C, VDD=1.8V ~ 5.5V, VSS=0V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Detection Level	V <sub>LVR</sub>	T <sub>A</sub> = - 10 °C to + 55 °C	1.71	1.80	1.89	V
Hysteresis	ΔV	-	-	25	100	mV
LVR Current	I <sub>BL</sub>	VDD=3V, T <sub>A</sub> = 25 °C	-	0.9	1.5	uA

**Table 7.6** Low Current LVR Characteristics

## 7.7 High Frequency Internal RC Oscillator Characteristics

(T<sub>A</sub>=-40°C ~ +85°C, VDD=1.8V ~ 5.5V, VSS=0V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units	
Frequency	f <sub>HFIRC</sub>	VDD = 2.0V – 5.5V	–	8	–	MHz	
Tolerance	–	T <sub>A</sub> = -10 °C to + 55°C	With 0.1uF bypass capacitor	-2.0	–	+2.0	%
		T <sub>A</sub> = - 20 °C to + 85°C		-3.0	–	+3.0	
		T <sub>A</sub> = - 40 °C to + 85°C		-4.0	–	+4.0	
		T <sub>A</sub> = -10 °C to + 55°C (User trim, Using only E-PGM +)		-1.0	–	+1.0	
Clock duty ratio	TOD	–	40	50	60	%	
Stabilization Time	t <sub>HFS</sub>	–	–	–	100	us	
HFIRC Current	I <sub>HFIRC</sub>	Enable	–	0.2	–	mA	
		Disable	–	–	0.1	uA	

**Table 7.7** High Frequency Internal RC Oscillator Characteristics

### NOTE)

1. User Trimming means the calibration of HFIRC frequency. Using E-PGM +.
2. To ensure ±1.0% tolerance of HFIRC frequency, it is necessary to do User Trimming.
3. Guaranteed by design, but might be On-Board programming after SMT process.  
(HFIRC Calibration with high temperature can cause the shift of the frequency, be sure to calibrate Enough to cool to near room temperature after SMT process)

## 7.8 Low Frequency Internal RC Oscillator Characteristics

(T<sub>A</sub>=-40°C ~ +85°C, VDD=1.8V ~ 5.5V, VSS=0V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units	
Frequency	f <sub>LFIRC</sub>	VDD = 2.0V – 5.5V	–	32	–	kHz	
Tolerance	–	T <sub>A</sub> = -10 °C to + 55°C	With 0.1uF bypass capacitor	-5.0	–	+5.0	%
Clock duty ratio	TOD	–		40	50	60	
Stabilization Time	t <sub>LFS</sub>	–	–	–	1	ms	
LFIRC Current	I <sub>LFIRC</sub>	Enable	VDD=5V	–	5	–	uA
		Disable		–	–	0.1	

**Table 7.8** Low Frequency Internal RC Oscillator Characteristics

## 7.9 Internal Watch-Dog Timer RC Oscillator Characteristics

(T<sub>A</sub>=-40°C ~ +85°C, VDD=1.8V ~ 5.5V, VSS=0V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Frequency	f <sub>WDTRC</sub>	–	2	5	10	kHz
Stabilization Time	t <sub>WDTS</sub>	–	–	–	1	ms
WDTRC Current	I <sub>WDTRC</sub>	Enable	–	1	–	uA
		Disable	–	–	0.1	

**Table 7.9** Internal WDTRC Oscillator Characteristics

### 7.10 LCD Voltage Characteristics

(T<sub>A</sub>= -40°C ~ +85°C, VDD=2.0V ~ 5.5V, VSS= 0V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units	
LCD Voltage	V <sub>LC3</sub>	Voltage booster enabled, 1/2 bias	Typx0.93	1.0+(Nx0.05)	Typx1.07	V	
		Voltage booster enabled, 1/3 and 1/4 bias	Typx0.93	Typx1.07	0.75		
					0.79		
					0.83		
					0.86		
					0.90		
					0.94		
					0.98		
					1.01		
					1.05		
					1.09		
					1.13		
					1.16		
					1.20		
1.24							
1.28							
1.31							
LCD Mid Bias Voltage	V <sub>LC0/1/2</sub>	Voltage booster enabled, 1/2 bias, No panel load, VDD=3V	Typx0.9	2xVLC3	Typx1.1	V	
	V <sub>LC0/1</sub>	Voltage booster enabled, 1/3 bias, No panel load, VDD=3V	Typx0.9	3xVLC3	Typx1.1		
	V <sub>LC2</sub>	Voltage booster enabled, 1/3 bias, No panel load, VDD=3V	Typx0.9	2xVLC3	Typx1.1		
	V <sub>LC0</sub>	Voltage booster enabled, 1/4 bias, No panel load, VDD=3V	Typx0.9	4xVLC3	Typx1.1		
	V <sub>LC1</sub>	Voltage booster enabled, 1/4 bias, No panel load, VDD=3V	Typx0.9	3xVLC3	Typx1.1		
	V <sub>LC2</sub>	Voltage booster enabled, 1/4 bias, No panel load, VDD=3V	Typx0.9	2xVLC3	Typx1.1		
	V <sub>LC1</sub>	Voltage booster disabled, LCD dividing resistor, VDD=2.7V to 5.5V, 1/4 bias, LCD clock = 0Hz, V <sub>LC0</sub> =VDD	Typ-0.2	0.75xVDD	Typ+0.2	V	
	V <sub>LC2</sub>	Voltage booster disabled, LCD dividing resistor, VDD=2.7V to 5.5V, 1/4 bias, LCD clock = 0Hz, V <sub>LC0</sub> =VDD	Typ-0.2	0.5xVDD	Typ+0.2		
V <sub>LC3</sub>	Voltage booster disabled, LCD dividing resistor, VDD=2.7V to 5.5V, 1/4 bias, LCD clock = 0Hz, V <sub>LC0</sub> =VDD	Typ-0.2	0.25xVDD	Typ+0.2			
LCD Driver Output Impedance	R <sub>LO</sub>	V <sub>LCD</sub> =3V, I <sub>LOAD</sub> =±10uA	–	5	10	kΩ	
LCD Bias Dividing Resistor	R <sub>LCD1</sub>	Internal resistor mode, T <sub>A</sub> = 25°C	20	30	40	kΩ	
	R <sub>LCD2</sub>		40	60	80		
	R <sub>LCD3</sub>		80	120	160		
LCD Block Current	I <sub>LCD</sub>	Voltage booster mode, VDD=3V, V <sub>LCD</sub> =3.15V, 1/3Bias	–	3	6	uA	

**Table 7.10** LCD Voltage Characteristics

**NOTE)**

- Where N is the value of LCDCCR register (N = 0 to 15).

## 7.11 DC Characteristics

(T<sub>A</sub>= -40°C ~ +85°C, VDD=1.8V ~ 5.5V, VSS= 0V, f<sub>XIN</sub>= 12MHz)

Parameter	Symbol	Conditions	Min	Typ	Max	Units	
Input High Voltage	V <sub>IH1</sub>	P32-P36, P4, P5, P6, RESETB	0.8VDD	–	VDD	V	
	V <sub>IH2</sub>	All input pins except V <sub>IH1</sub>	0.7VDD	–	VDD		
Input Low Voltage	V <sub>IL1</sub>	P32-P36, P4, P5, P6, RESETB	–	–	0.2VDD	V	
	V <sub>IL2</sub>	All input pins except V <sub>IL1</sub>	–	–	0.3VDD		
Output High Voltage	V <sub>OH</sub>	VDD=4.5V, I <sub>OH</sub> = – 2mA; All output ports except REM pin	VDD-1.0	–	–	V	
Output Low Voltage	V <sub>OL</sub>	VDD=4.5V, I <sub>OL</sub> =15mA; All output ports except REM pin	–	–	1.0	V	
Output High Current	I <sub>OH</sub>	VDD=4.5V, V <sub>OH</sub> = 3.5V; All output ports except REM pin	-2	–	–	mA	
Output Low Current	I <sub>OL</sub>	VDD=4.5V, V <sub>OL</sub> = 1.0V; All output ports except REM pin	15	–	–	mA	
REM Output High Current	I <sub>OH1</sub>	VDD=3.0V, V <sub>OH</sub> =2.0V, ROTS=1	–	-10	-5	mA	
REM Output Low Current	I <sub>OL1</sub>	VDD=3.0V, V <sub>OL</sub> =1.0V, TA=25°C	ROTS=1	2.5	5.0	–	mA
	I <sub>OL2</sub>		ROTS=0, RIOL=3	470	630	–	
Input high leakage current	I <sub>IH</sub>	All Input ports	–	–	1	uA	
Input low leakage current	I <sub>IL</sub>	All Input ports	-1	–	–	uA	
Pull-up resistor	R <sub>PU1</sub>	VI=0V, TA=25°C, All Input ports	VDD=5V	50	80	110	kΩ
			VDD=3V	100	155	210	
	R <sub>PU2</sub>	VI=0V, TA=25°C, RESETB	VDD=5V	150	250	400	
			VDD=3V	300	500	700	
OSC feedback resistor	R <sub>X1</sub>	XIN=VDD, XOUT=VSS TA=25°C, VDD=5V FBS = 0 (Configure Option 2 : 3FH)	600	1200	2000	kΩ	
		XIN=VDD, XOUT=VSS TA=25°C, VDD=5V FBS = 1 (Configure Option 2 : 3FH)	250	500	750		
	R <sub>X2</sub>	SXIN=VDD, SXOUT=VSS TA=25°C, VDD=5V	2500	5000	10000	kΩ	

Table 7.11 DC Characteristics

### 7.11 DC Characteristics (Continued)

(T<sub>A</sub>= -40°C ~ +85°C, VDD=1.8V ~ 5.5V, VSS= 0V, f<sub>XIN</sub>= 12MHz)

Parameter	Symbol	Conditions	Min	Typ	Max	Units	
Supply current	I <sub>DD1</sub> (Run)	f <sub>XIN</sub> =12MHz, VDD=5V±10%	–	3.0	6.0	mA	
		f <sub>XIN</sub> =8MHz, VDD=3V±10%	–	2.0	4.0		
		f <sub>HFIRC</sub> =8MHz, VDD=5V±10%	–	2.0	4.0		
	I <sub>DD2</sub> (Idle)	f <sub>XIN</sub> =12MHz, VDD=5V±10%	–	2.0	4.0	mA	
		f <sub>XIN</sub> =8MHz, VDD=3V±10%	–	1.0	2.0		
		f <sub>HFIRC</sub> =8MHz, VDD=5V±10%	–	1.0	2.0		
	I <sub>DD3</sub> (Run)	f <sub>SUB</sub> =32.768kHz	VDD=3V±10%, TA=25°C	–	90.0	180.0	uA
		f <sub>LFIRC</sub> =32kHz		–	90.0	180.0	
	I <sub>DD4</sub> (Idle)	f <sub>SUB</sub> =32.768kHz	VDD=3V±10%, TA=25°C	–	4.0	8.0	uA
		f <sub>LFIRC</sub> =32kHz		–	6.0	12.0	
I <sub>DD5</sub>	Stop, VDD=3V±10%, TA=25°C		–	0.5	2.7	uA	

**Table 7.11** DC Characteristics (Continued)

**NOTE)**

1. Where the f<sub>XIN</sub> is an external main oscillator, the f<sub>SUB</sub> is an external sub oscillator, the f<sub>HFIRC</sub> is an internal high frequency RC oscillator, the f<sub>LFIRC</sub> is an internal low frequency RC oscillator and the fx is the selected system clock.
2. All supply current items don't include the current of an internal Watch-dog timer RC (WDTRC) oscillator and a peripheral block.
3. All supply current items include the current of the power-on reset (POR) block.

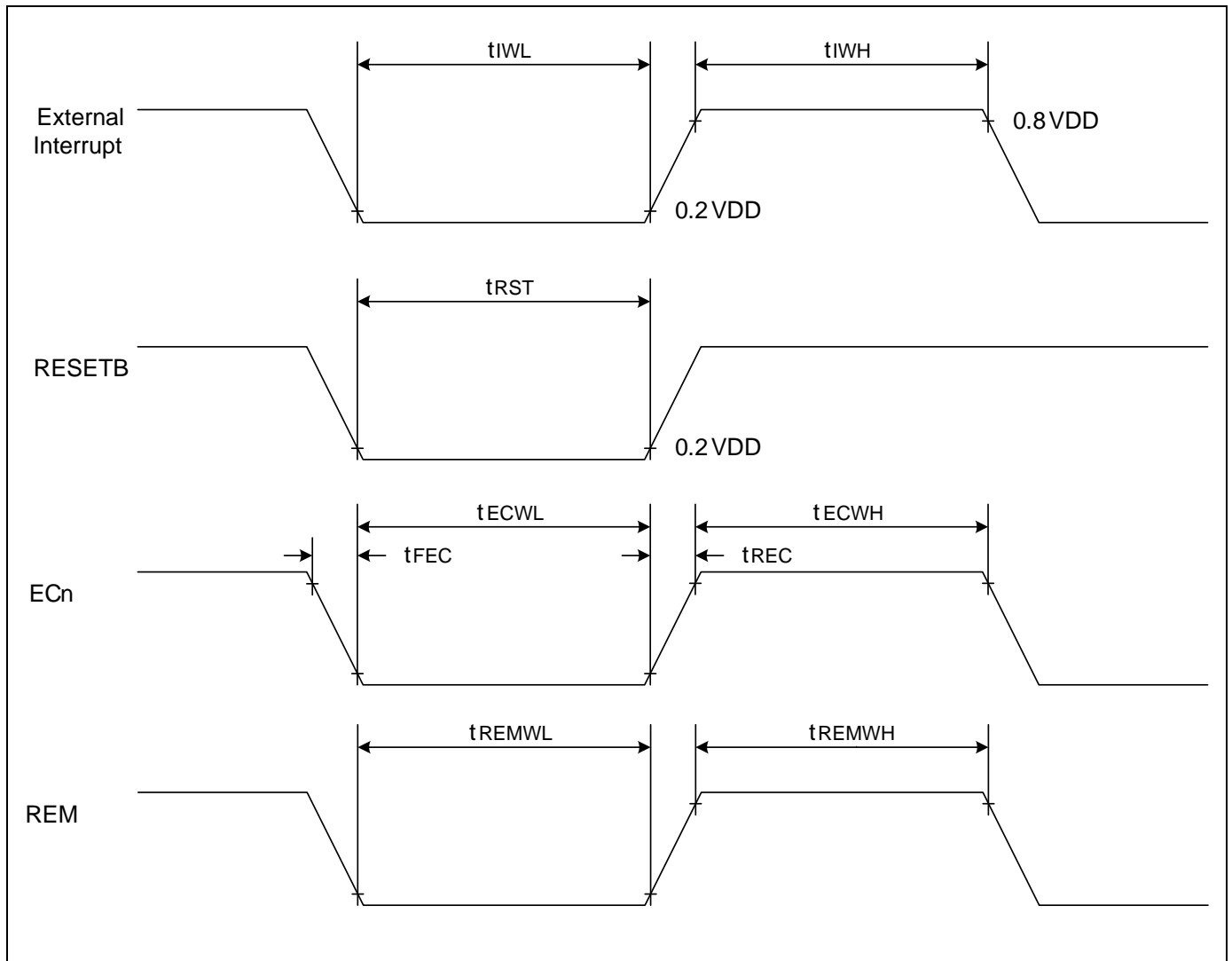


### 7.12 AC Characteristics

( $T_A = -40^{\circ}\text{C} \sim +85^{\circ}\text{C}$ ,  $V_{DD} = 1.8\text{V} \sim 5.5\text{V}$ )

Parameter	Symbol	Conditions	Min	Typ	Max	Units
RESETB input low width	$t_{RST}$	$V_{DD} = 5\text{V}$	10	–	–	us
Interrupt Input High, Low width	$t_{IWH}, t_{IWL}$	All interrupts, $V_{DD} = 5\text{V}$	200	–	–	ns
External Counter Input High, Low Pulse Width	$t_{ECWH}, t_{ECWL}$	$EC_n, V_{DD} = 5\text{V}$ ( $n=0, 2$ )	200	–	–	
External Counter Transition Time	$t_{REC}, t_{FEC}$	$EC_n, V_{DD} = 5\text{V}$ ( $n=0, 2$ )	20	–	–	
REM port High, Low width	$t_{REMWH}, t_{REMWL}$	REM, $V_{DD} = 5\text{V}$	5	–	–	us

**Table 7.12** AC Characteristics



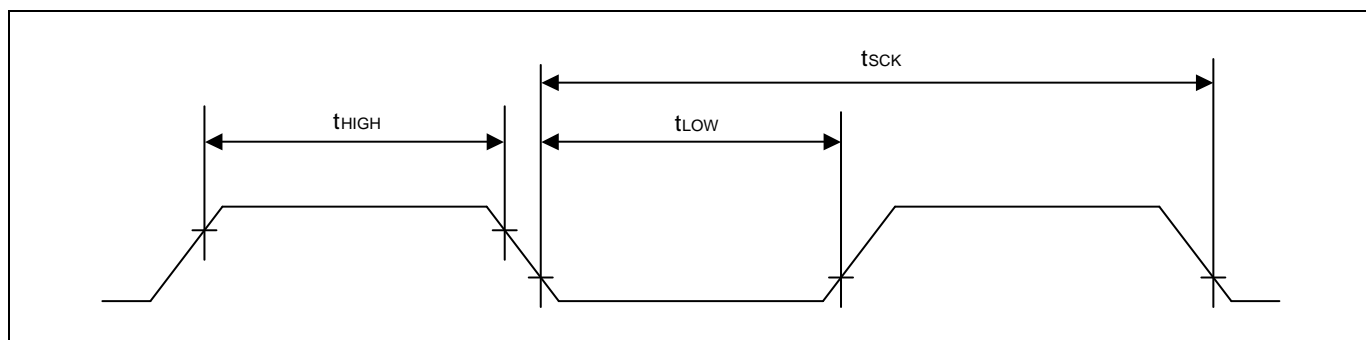
**Figure 7.2** AC Timing

### 7.13 UART TIMING CHARACTERISTICS

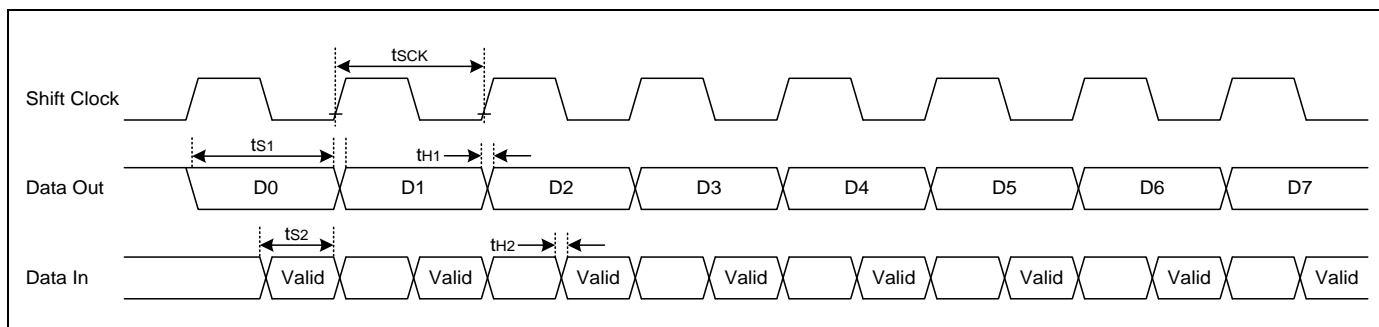
( $T_A = -40^{\circ}\text{C} \sim +85^{\circ}\text{C}$ ,  $V_{DD} = 1.8\text{V} \sim 5.5\text{V}$ ,  $f_{XIN} = 11.1\text{MHz}$ )

Parameter	Symbol	Min	Typ	Max	Units
Serial port clock cycle time	$t_{SCK}$	1250	$t_{CPU} \times 16$	1650	ns
Output data setup to clock rising edge	$t_{S1}$	590	$t_{CPU} \times 13$	—	
Clock rising edge to input data valid	$t_{S2}$	—	—	590	
Output data hold after clock rising edge	$t_{H1}$	$t_{CPU} - 50$	$t_{CPU}$	—	
Input data hold after clock rising edge	$t_{H2}$	0	—	—	
Serial port clock High, Low level width	$t_{HIGH}, t_{LOW}$	470	$t_{CPU} \times 8$	970	

**Table 7.13** UART TIMING CHARACTERISTICS



**Figure 7.3** Waveform for UART Timing



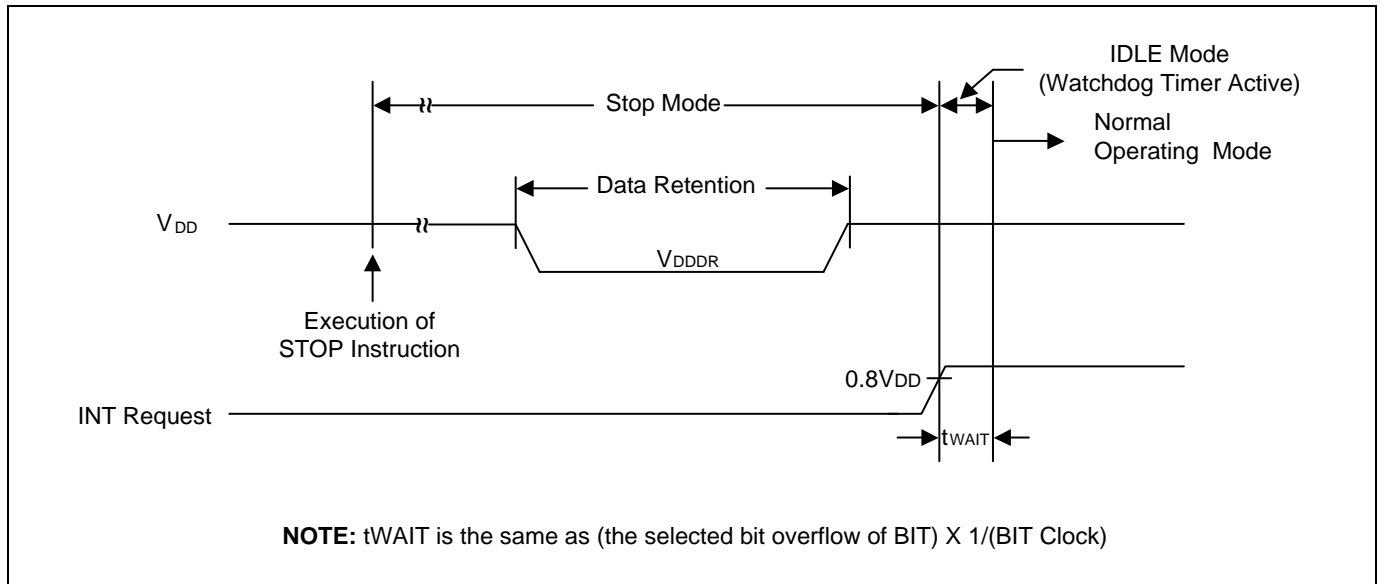
**Figure 7.4** Timing Waveform for UART Module

### 7.14 Data Retention Voltage in Stop Mode

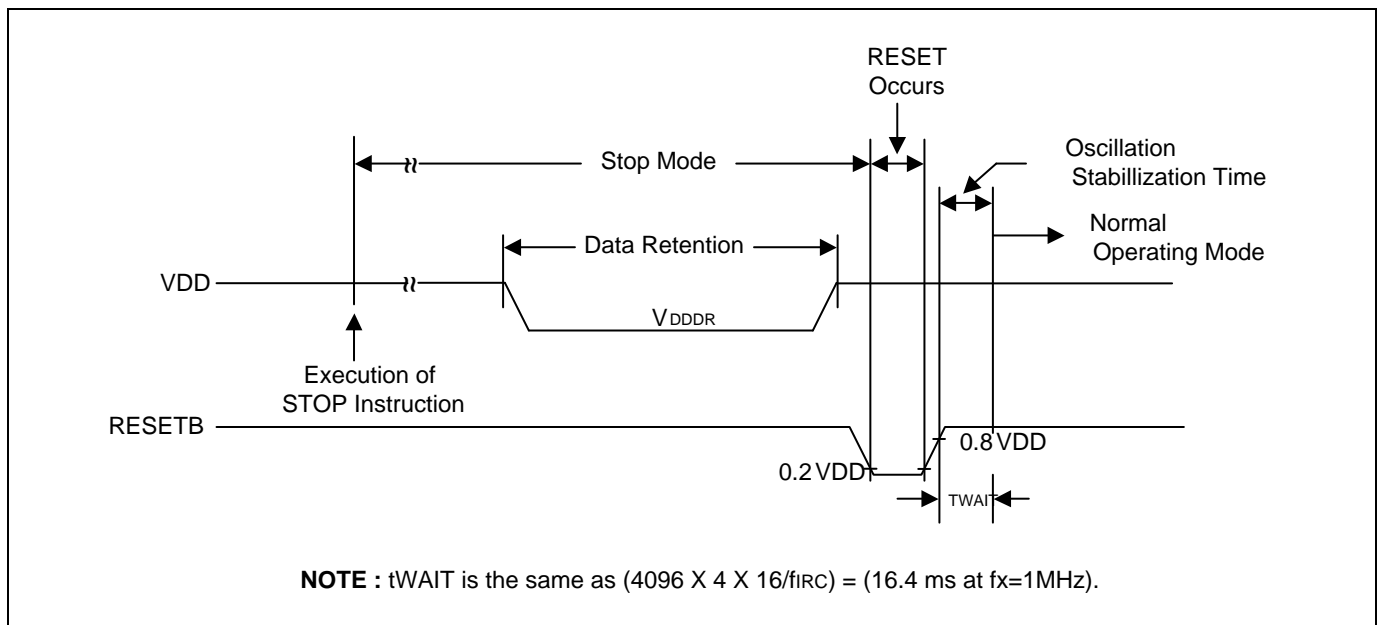
( $T_A = -40^{\circ}\text{C} \sim +85^{\circ}\text{C}$ ,  $V_{DD} = 1.8\text{V} \sim 5.5\text{V}$ )

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Data retention supply voltage	$V_{DDDR}$	–	1.0	–	5.5	V
Data retention supply current	$I_{DDDR}$	$V_{DDDR} = 1.0\text{V}$ ( $T_A = 25^{\circ}\text{C}$ ), Stop mode	–	–	1	$\mu\text{A}$

**Table 7.14** Data Retention Voltage in Stop Mode



**Figure 7.5** Stop Mode Release Timing when Initiated by an Interrupt



**Figure 7.6** Stop Mode Release Timing when Initiated by RESETB

### 7.15 Internal Flash Rom Characteristics

(T<sub>A</sub>=-40°C ~ +85°C, VDD=1.8V ~ 5.5V, VSS= 0V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Sector Write Time	t <sub>FSW</sub>	–	–	2.5	2.7	ms
Sector Erase Time	t <sub>FSE</sub>	–	–	2.5	2.7	
Hard-Lock Time	t <sub>FHL</sub>	–	–	2.5	2.7	
Page Buffer Reset Time	t <sub>FBR</sub>	–	–	–	5	us
Flash Programming Voltage	V <sub>PGM</sub>	–	2.0	–	5.5	V
Flash Programming Frequency	f <sub>PGM</sub>	–	0.4	–	–	MHz
Endurance of Write/Erase	N <sub>FWE</sub>	Sector 0 to 379	–	–	10,000	Times
		Sector 380 to 383 (256 bytes)	–	–	100,000	
Flash Data Retention Time	t <sub>RT</sub>	–	10	–	–	Years

**Table 7.15** Internal Flash Rom Characteristics

**NOTE)**

1. During a flash operation, SCLK[1:0] of SCCR must be set to “00” or “01” (HF INT-RC OSC or Main XTAL for system clock).

### 7.16 Input/Output Capacitance

(T<sub>A</sub>=-40°C ~ +85°C, VDD=0V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Capacitance	C <sub>IN</sub>	f <sub>x</sub> =1MHz Unmeasured pins are connected to Vss	–	–	10	pF
Output Capacitance	C <sub>OUT</sub>					
I/O Capacitance	C <sub>IO</sub>					

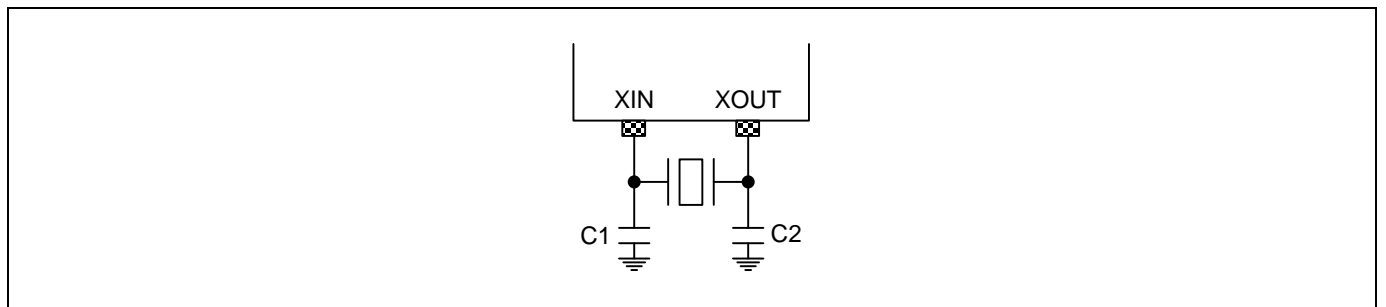
**Table 7.16** Input/Output Capacitance

### 7.17 Main Clock Oscillator Characteristics

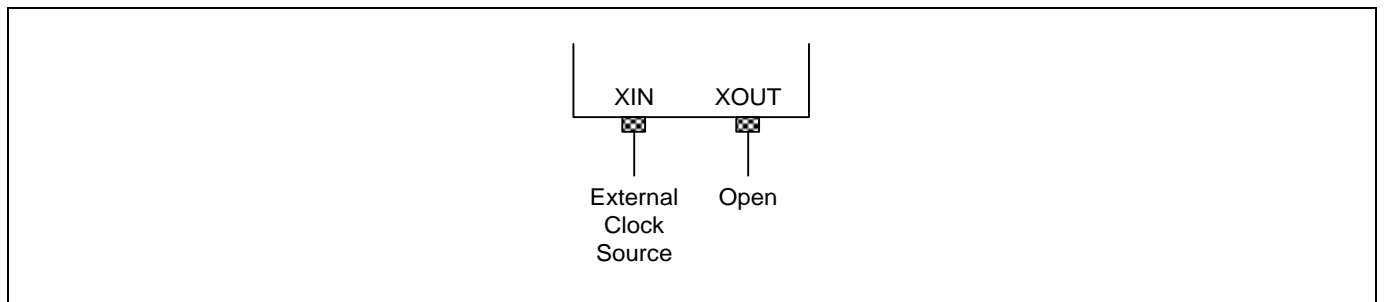
( $T_A = -40^{\circ}\text{C} \sim +85^{\circ}\text{C}$ ,  $V_{DD} = 1.8\text{V} \sim 5.5\text{V}$ )

Oscillator	Parameter	Conditions	Min	Typ.	Max	Units
Crystal	Main oscillation frequency	2.0 V – 5.5 V	0.4	–	4.2	MHz
		2.4 V – 5.5 V	0.4	–	8.0	
		3.0 V – 5.5 V	0.4	–	12.0	
Ceramic Oscillator	Main oscillation frequency	1.8 V – 5.5 V	0.4	–	4.2	
		2.4 V – 5.5 V	0.4	–	8.0	
		3.0 V – 5.5 V	0.4	–	12.0	
External Clock	XIN input frequency	1.8 V – 5.5 V	0.4	–	4.2	MHz
		2.4 V – 5.5 V	0.4	–	8.0	
		3.0 V – 5.5 V	0.4	–	12.0	

**Table 7.17** Main Clock Oscillator Characteristics



**Figure 7.7** Crystal/Ceramic Oscillator



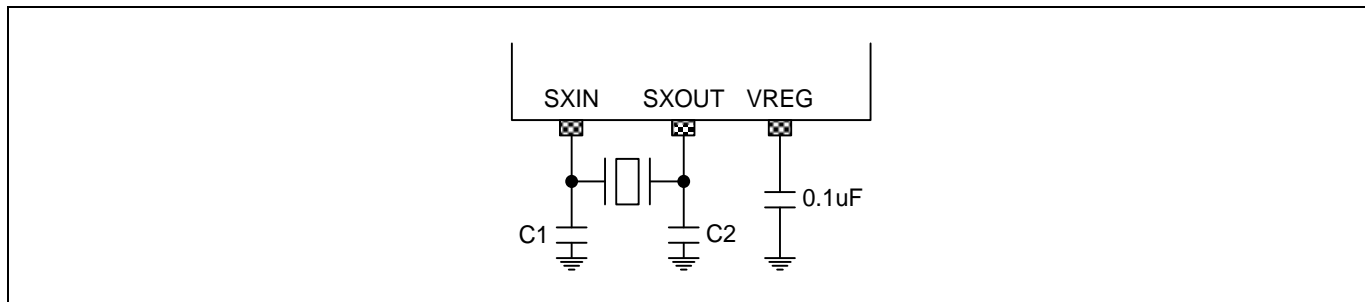
**Figure 7.8** External Clock

### 7.18 Sub Clock Oscillator Characteristics

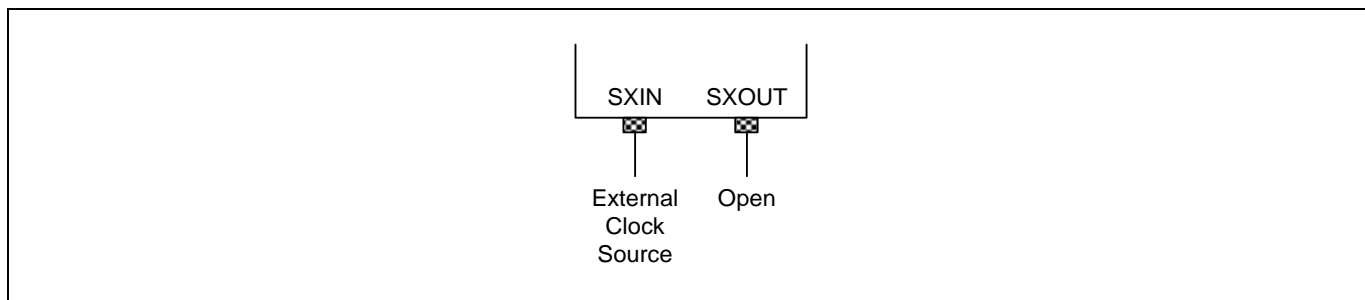
( $T_A = -40^{\circ}\text{C} \sim +85^{\circ}\text{C}$ ,  $V_{DD} = 1.8\text{V} \sim 5.5\text{V}$ )

Oscillator	Parameter	Conditions	Min	Typ.	Max	Units
Crystal	Sub oscillation frequency	1.8 V – 5.5 V	32	32.768	38	kHz
External Clock	SXIN input frequency		32	–	100	

**Table 7.18** Sub Clock Oscillator Characteristics



**Figure 7.9** Crystal Oscillator



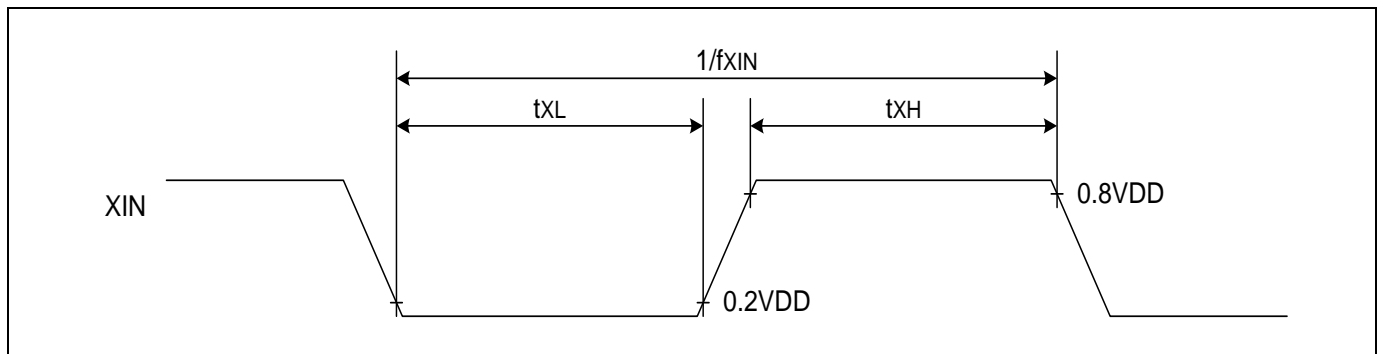
**Figure 7.10** External Clock

### 7.19 Main Oscillation Stabilization Characteristics

( $T_A = -40^\circ\text{C} \sim +85^\circ\text{C}$ ,  $V_{DD} = 1.8\text{V} \sim 5.5\text{V}$ )

Oscillator	Conditions	Min	Typ.	Max	Units
Crystal	$f_{XIN} \geq 1\text{ MHz}$ , $V_{DD} = 2.0\text{V} \sim 5.5\text{V}$ Oscillation stabilization occurs when $V_{DD}$ is equal to the minimum oscillator voltage range.	-	-	60	ms
Ceramic	$f_{XIN} \geq 1\text{ MHz}$ , $V_{DD} = 1.8\text{V} \sim 5.5\text{V}$ Oscillation stabilization occurs when $V_{DD}$ is equal to the minimum oscillator voltage range.	-	-	10	
External Clock	$f_{XIN} = 0.4\text{ to }12\text{ MHz}$ XIN input high and low width ( $t_{XL}$ , $t_{XH}$ )	42	-	1250	ns

**Table 7.19** Main Oscillation Stabilization Characteristics



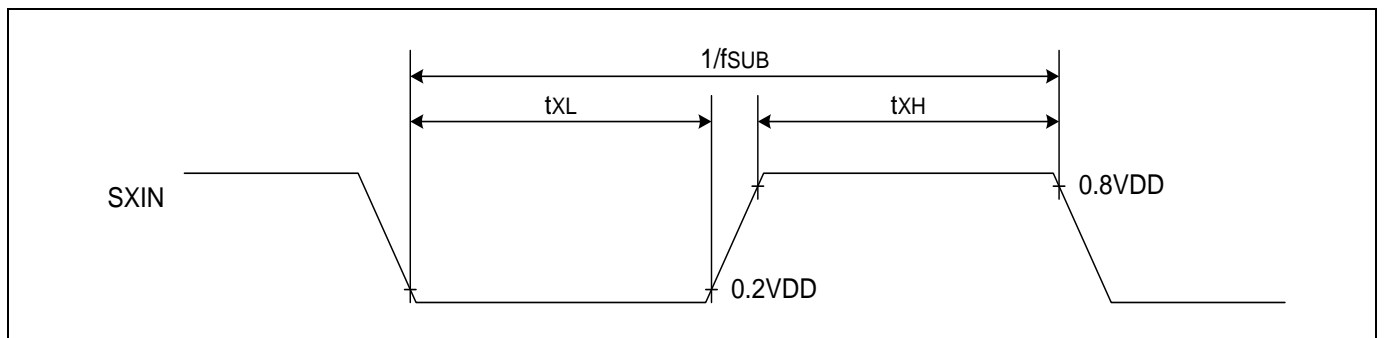
**Figure 7.11** Clock Timing Measurement at XIN

### 7.20 Sub Oscillation Stabilization Characteristics

( $T_A = -40^\circ\text{C} \sim +85^\circ\text{C}$ ,  $V_{DD} = 1.8\text{V} \sim 5.5\text{V}$ )

Oscillator	Conditions	Min	Typ.	Max	Units
Crystal	-	-	-	10	sec
	$V_{DD} = 3.0\text{V}$ , $T_A = 25^\circ\text{C}$	-	0.7	1.5	
External Clock	SXIN input high and low width ( $t_{XL}$ , $t_{XH}$ )	5	-	15	us

**Table 7.20** Sub Oscillation Stabilization Characteristics



**Figure 7.12** Clock Timing Measurement at SXIN

### 7.21 Operating Voltage Range

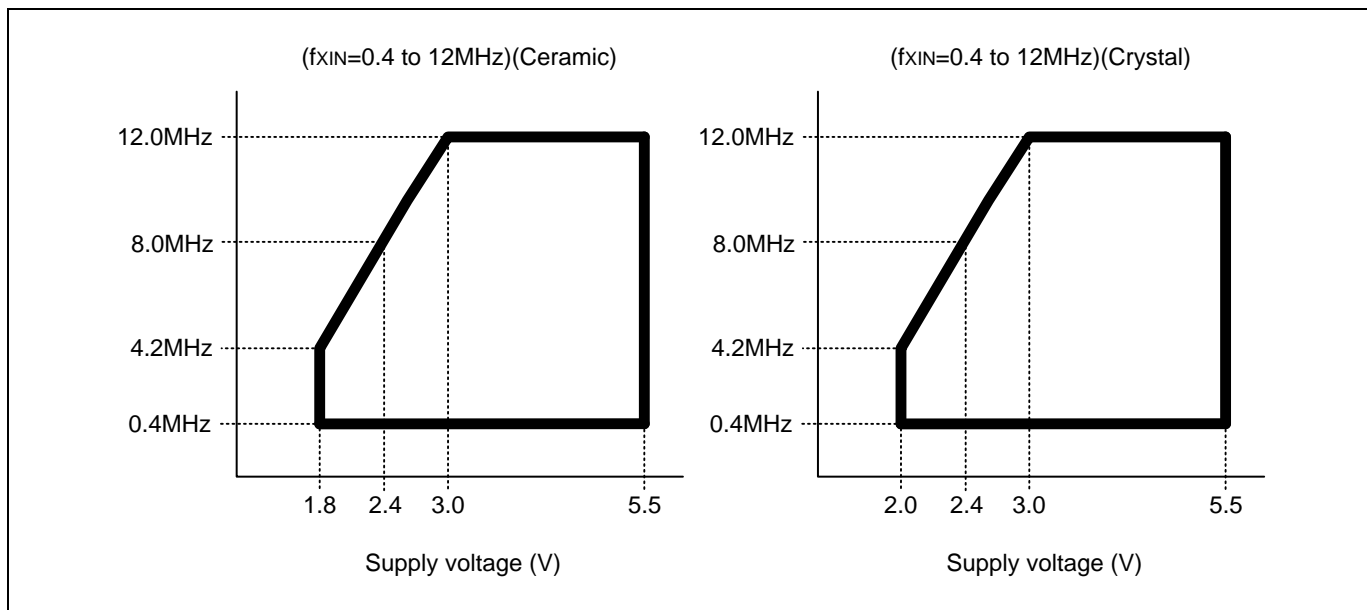


Figure 7.13 Operating Voltage Range (Main OSC)

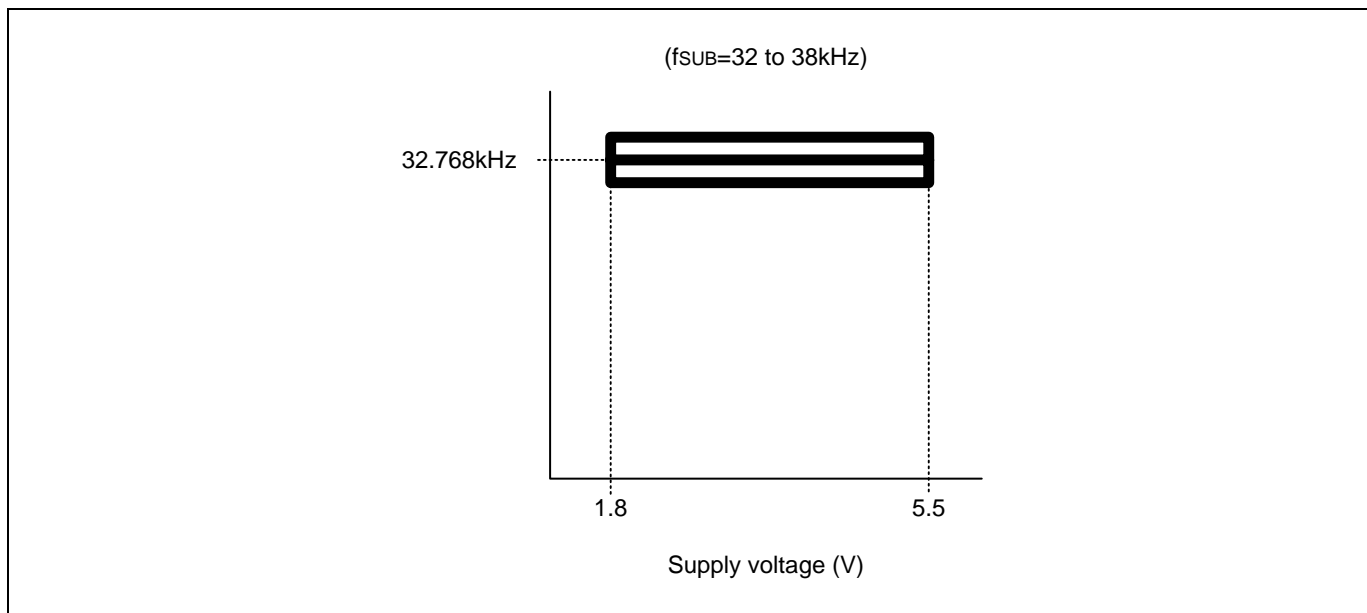


Figure 7.14 Operating Voltage Range (Sub OSC)



### 7.22 Recommended Circuit and Layout

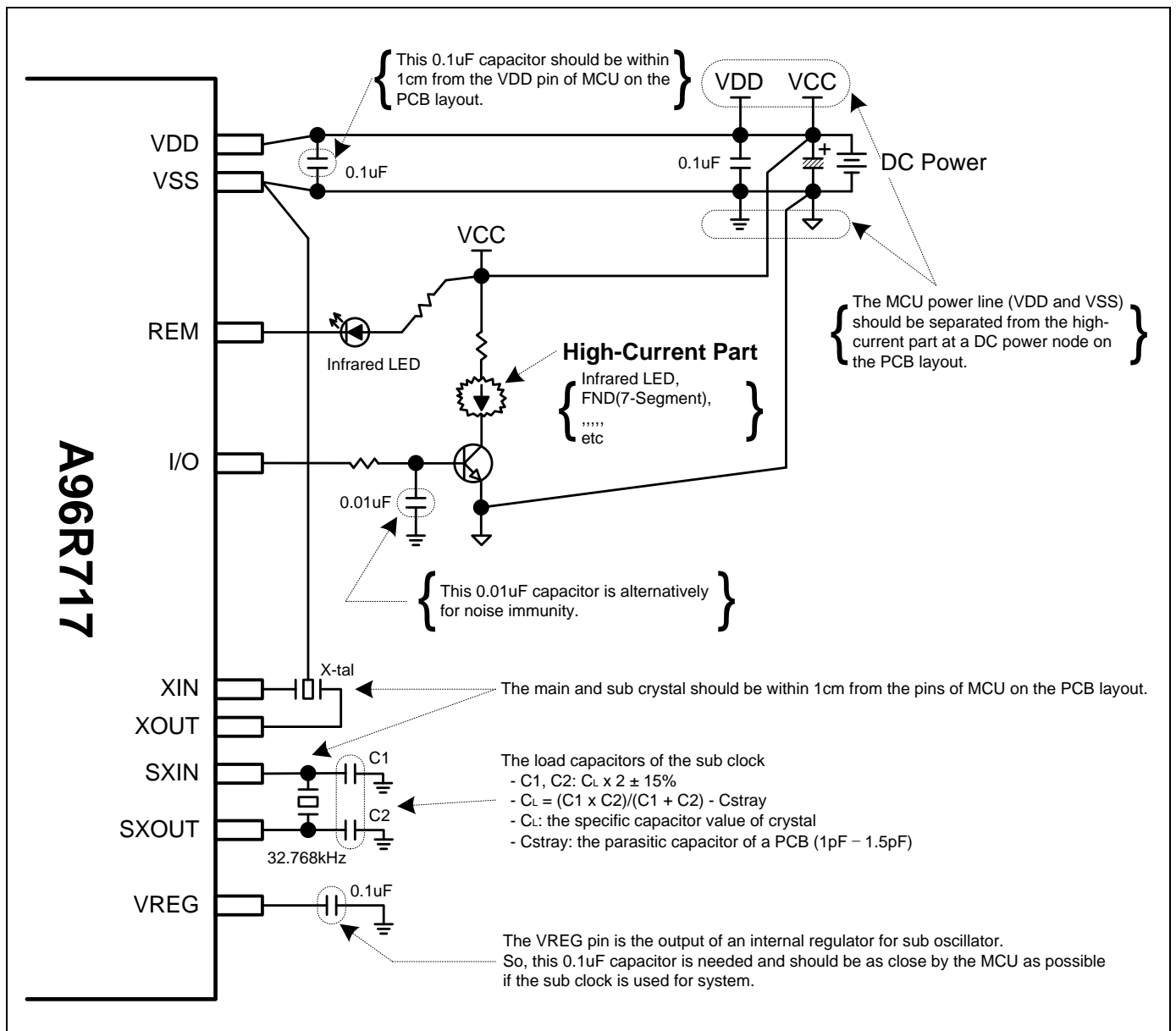


Figure 7.15 Recommended Circuit and Layout

### 7.23 Recommended Circuit for Remote controller

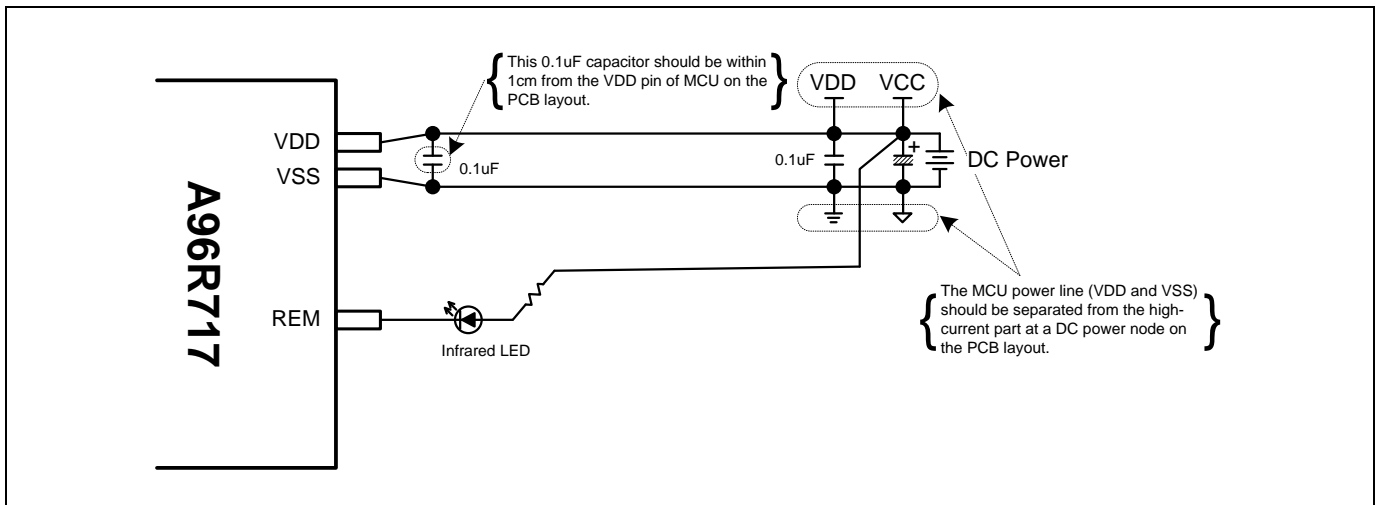


Figure 7.16 Recommended Circuit for Remote controller

### 7.24 Recommended Circuit and Layout with SMPS Power

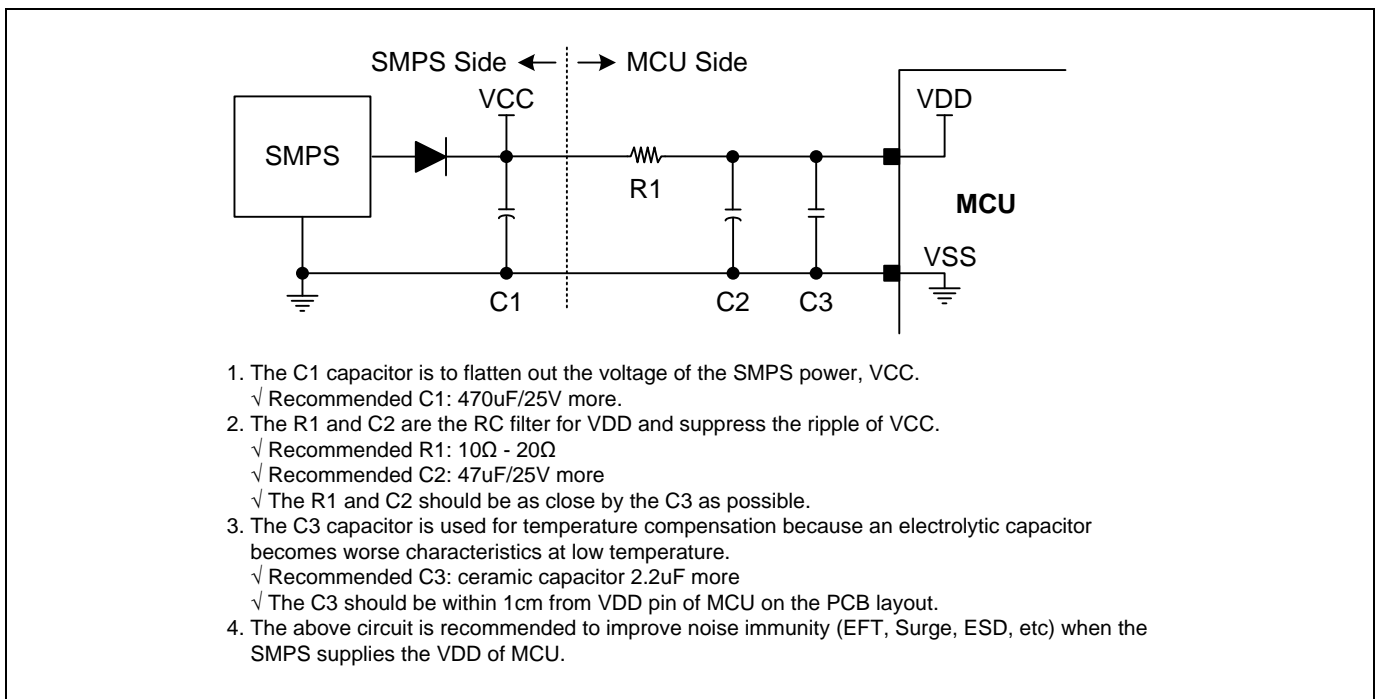


Figure 7.17 Recommended Circuit and Layout with SMPS Power

### 7.25 Typical Characteristics

These graphs and tables provided in this section are only for design guidance and are not tested or guaranteed. In graphs or tables some data are out of specified operating range (e.g. out of specified VDD range). This is only for information and devices are guaranteed to operate properly only within the specified range.

The data presented in this section is a statistical summary of data collected on units from different lots over a period of time. "Typical" represents the mean of the distribution while "max" or "min" represents (mean + 3σ) and (mean - 3σ) respectively where σ is standard deviation.

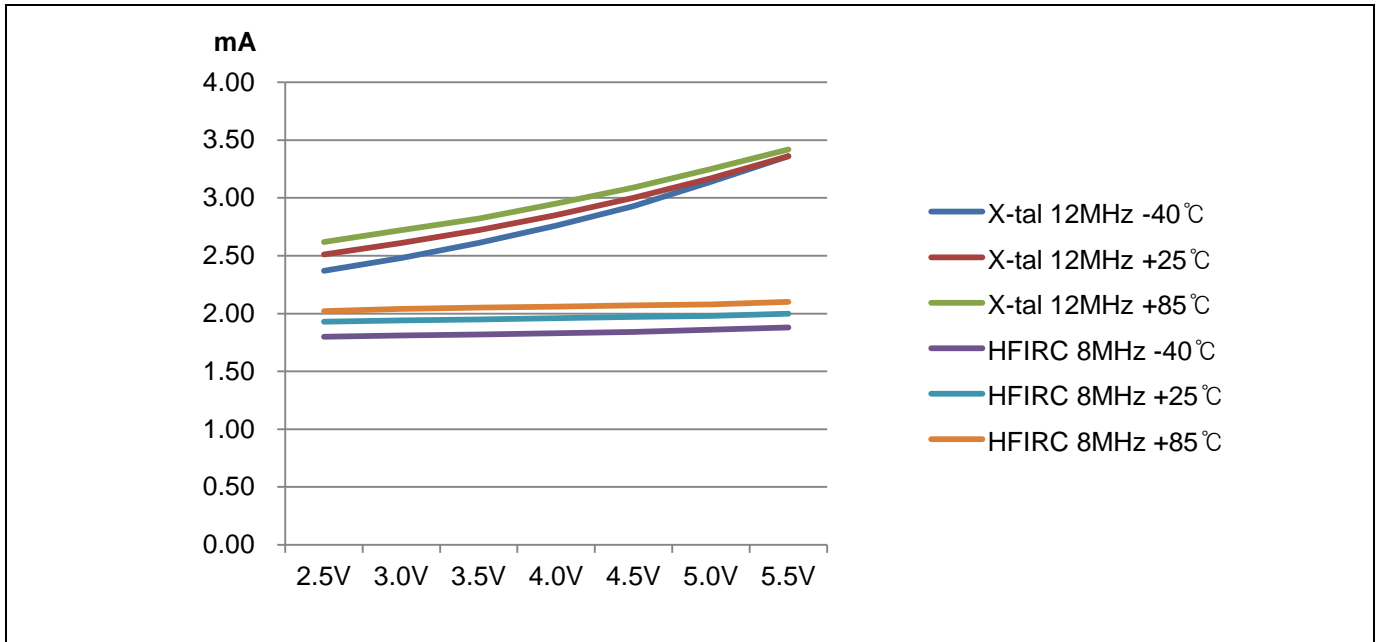


Figure 7.18 RUN (IDD1) Current

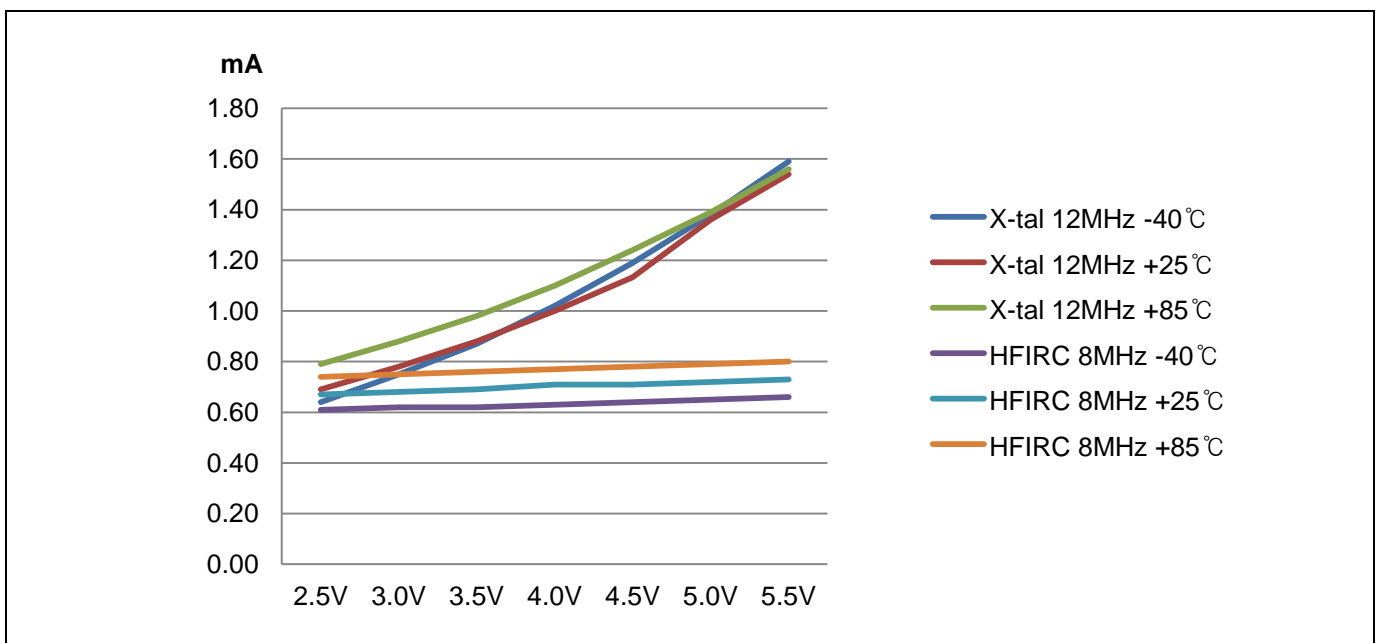


Figure 7.19 IDLE (IDD2) Current

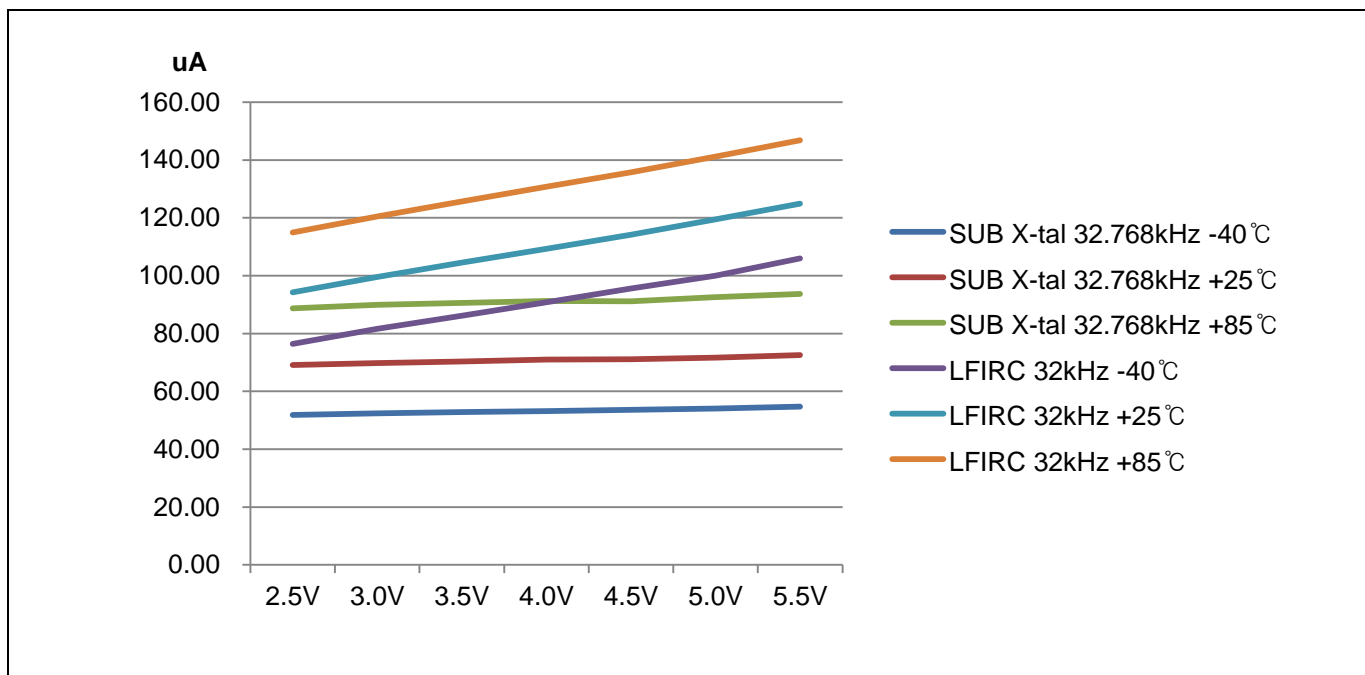


Figure 7.20 RUN (IDD3) Current

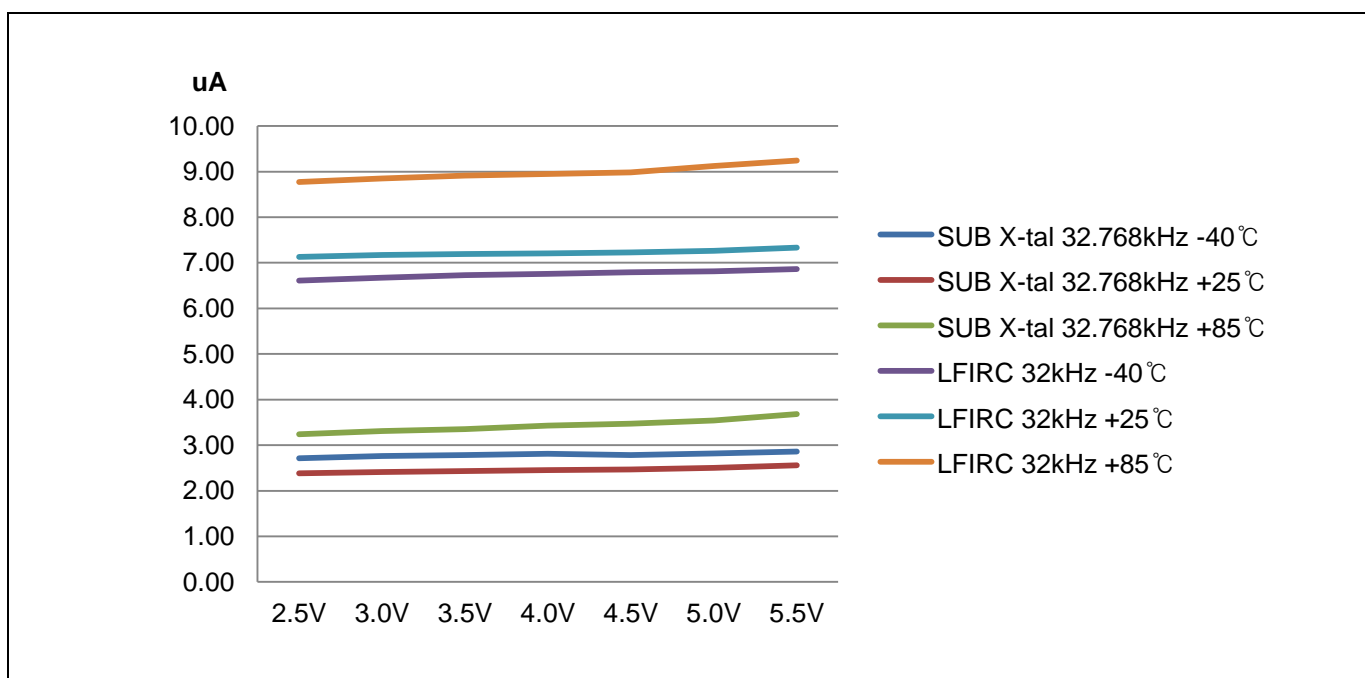


Figure 7.21 IDLE (IDD4) Current

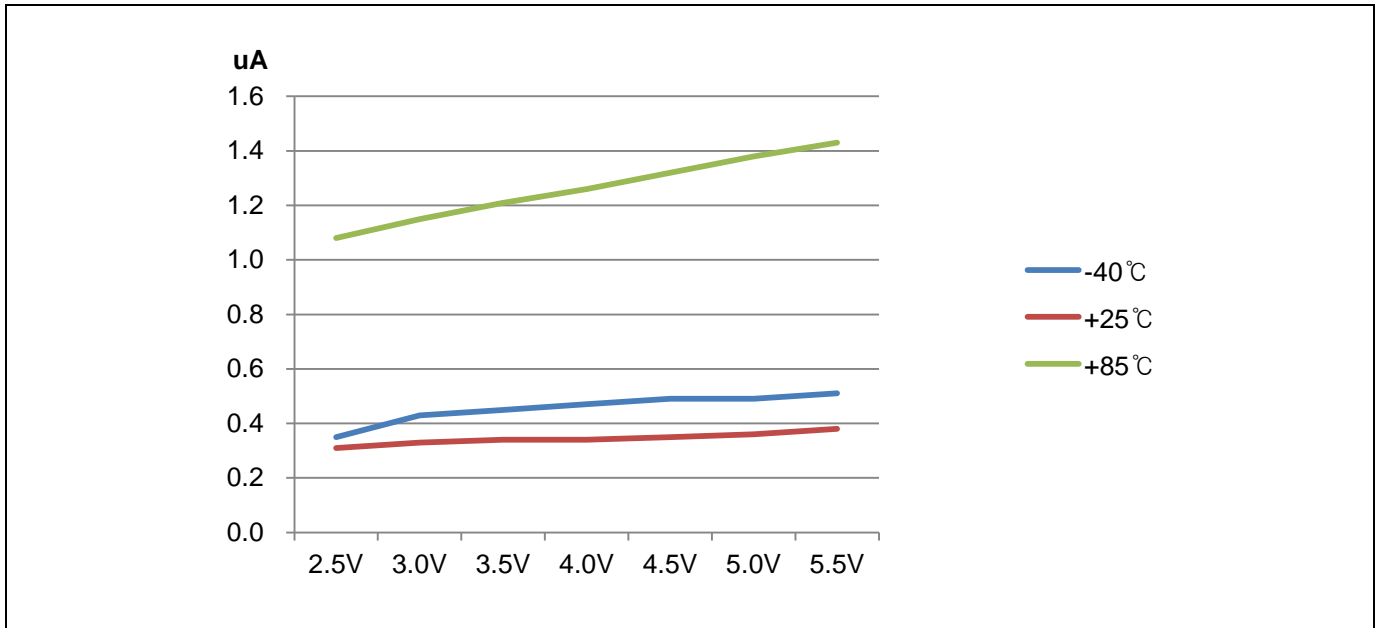


Figure 7.22 STOP (IDD5) Current

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